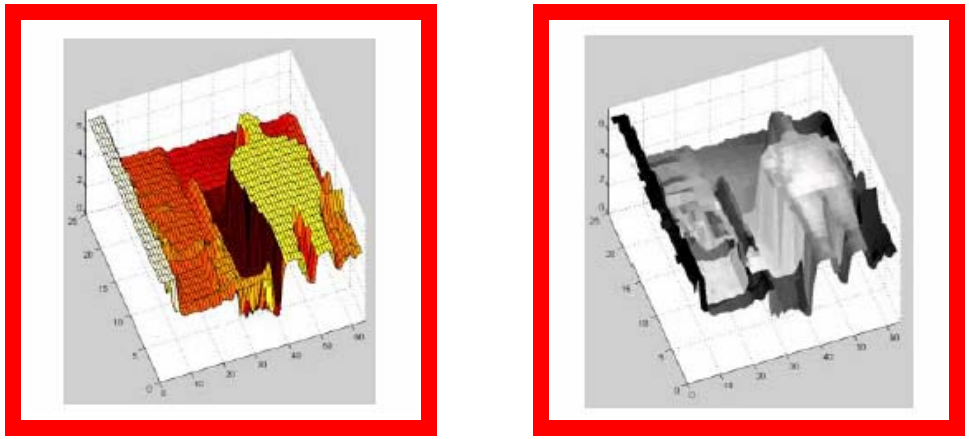
ORTHOGONALLY MODULATED CMOS READOUT INTEGRATED CIRCUIT FOR IMAGING APPLICATIONS



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Report Documentation Page

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ORTHOGONALLY MODULATED CMOS READOUT INTEGRATED CIRCUIT FOR IMAGING APPLICATIONS

- Introduction and motivation
- Contribution Phase I: Proof of principle
  - Orthogonal encoding readout system description
  - Prototype system design and verification
  - Conclusions
- Contribution Phase II: Improving the system performance
  - Readout cell improvements
  - Transimpedance amplifier integration
- Conclusion and brainstorm on further improvements

Read Out Integrated Circuit ROIC

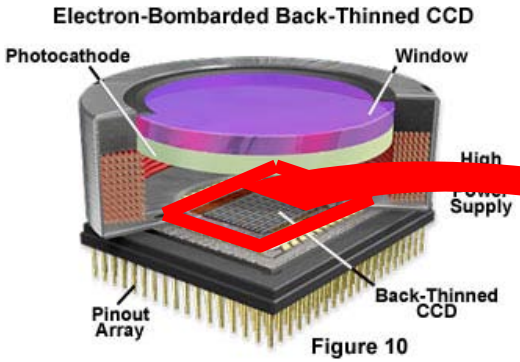
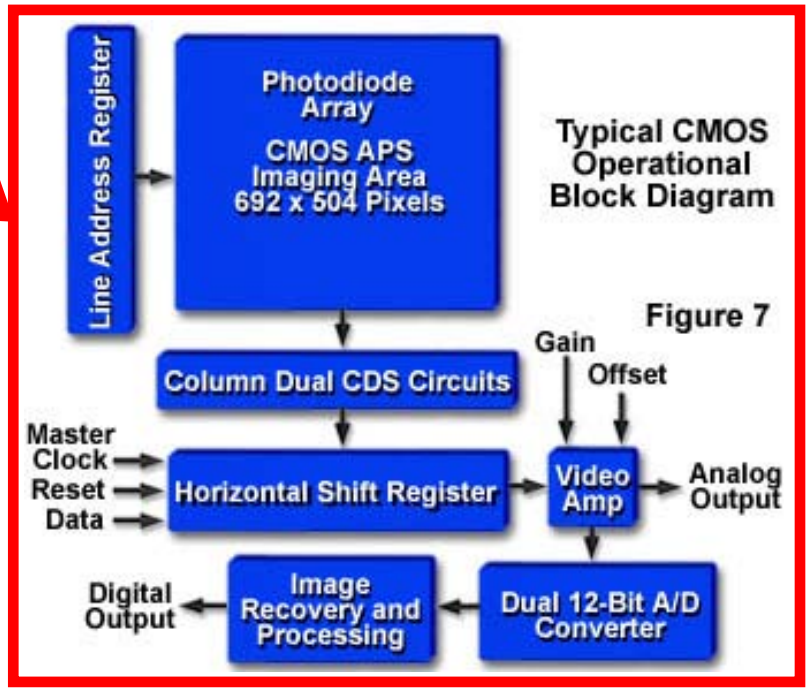


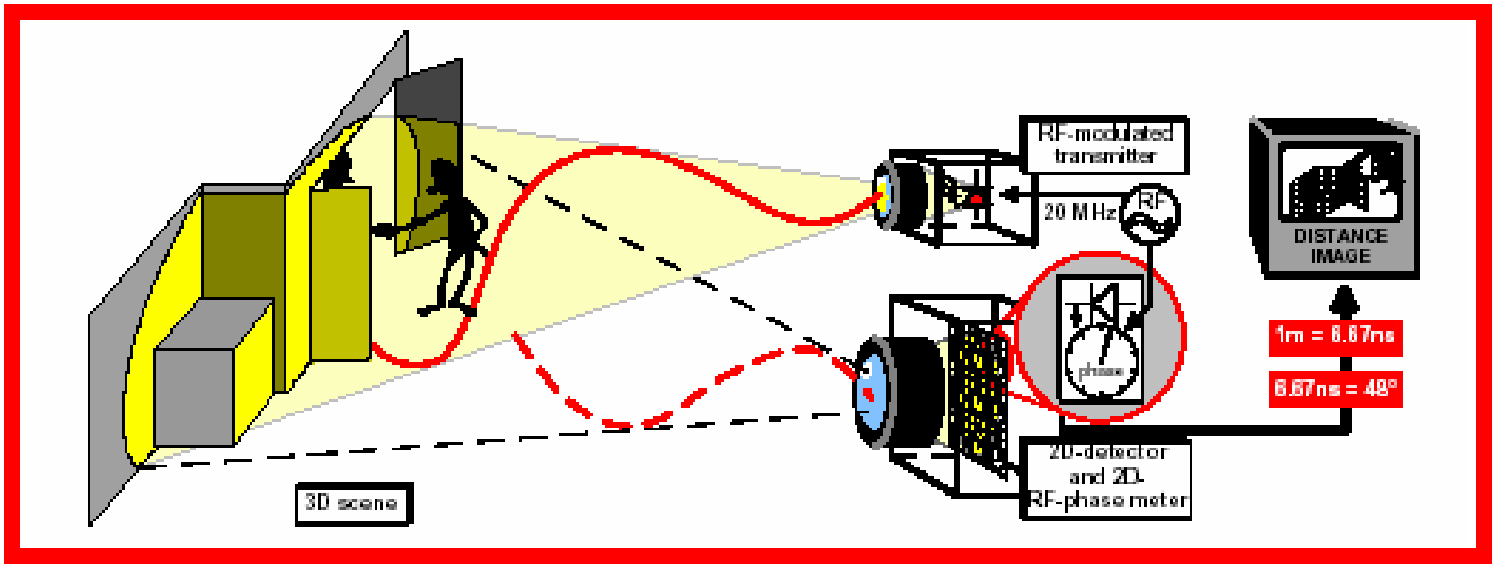
Figure 10

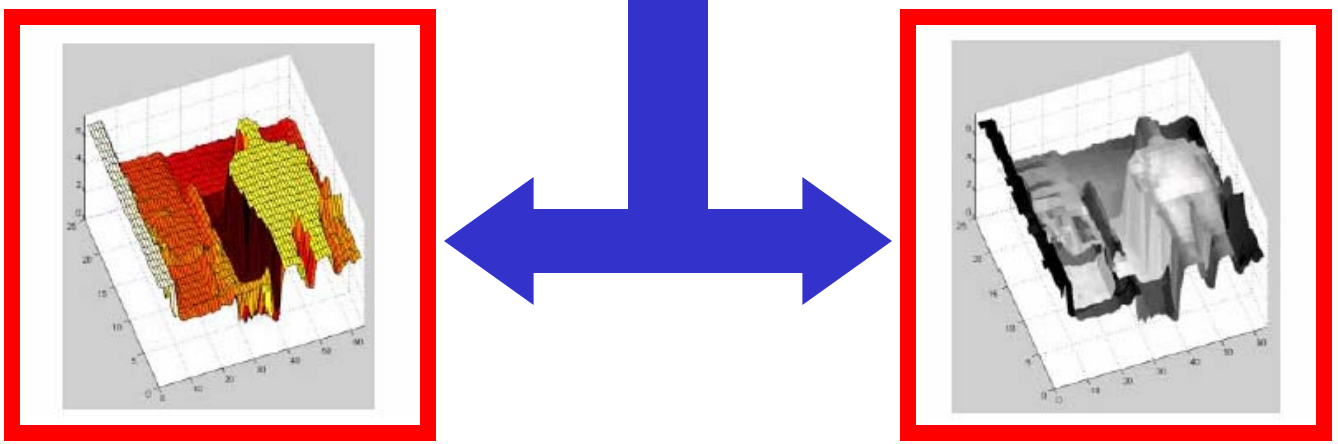


ROIC may include:

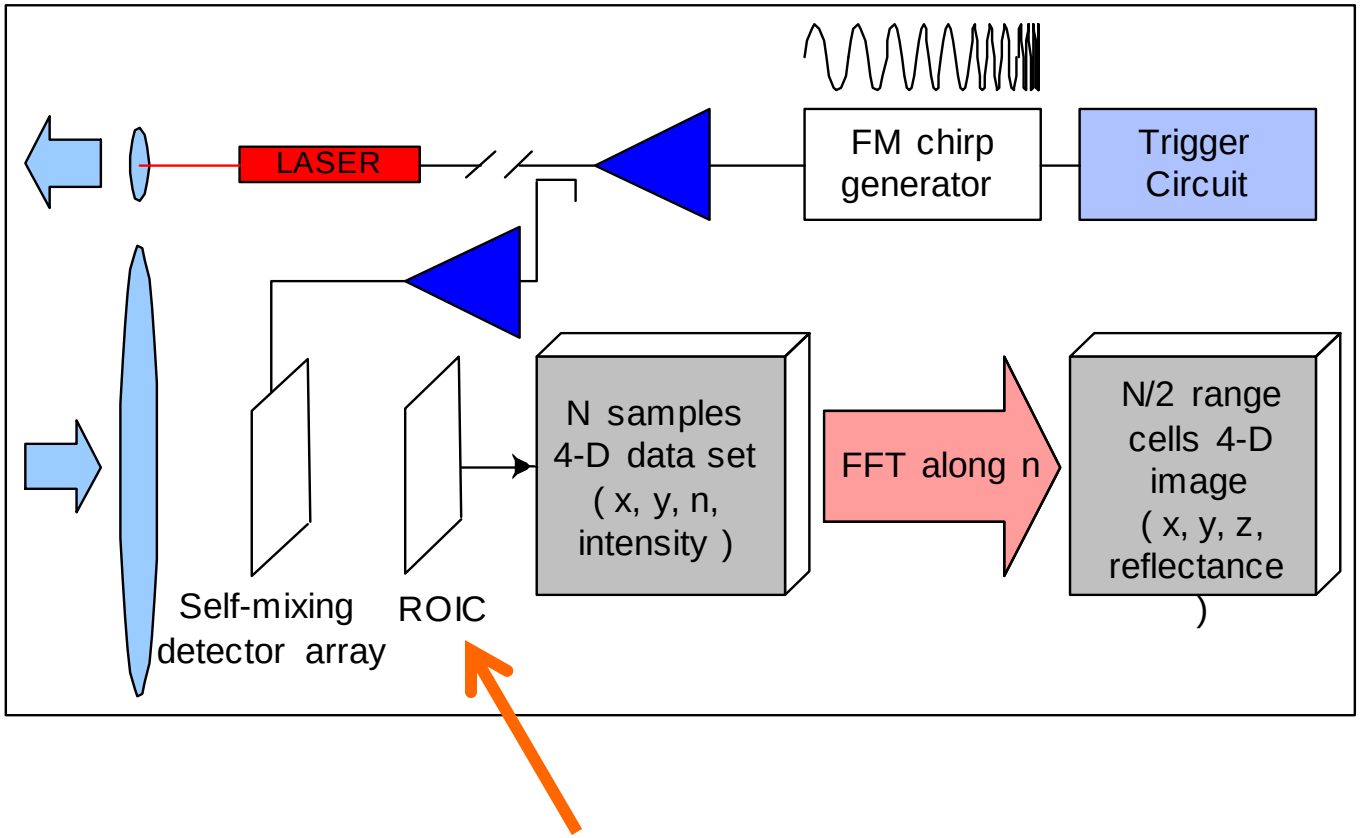
Amplifier electronics
Control signal generators
Analog-Digital Conversion
On-chip Digital Signal Processing

Distance information: a time of flight measurement





FM/CW LADAR system



Motivation: **Readout Integrated Circuit ROIC for active/passive imaging systems**

ORTHOGONALLY MODULATED CMOS READOUT INTEGRATED CIRCUIT FOR IMAGING APPLICATIONS

- Introduction and motivation
- **Contribution Phase I: Proof of principle**
  - **Orthogonal encoding readout system description**
  - **Prototype system design and verification**
  - **Conclusions**
- Contribution Phase II: Improving the system performance
  - Readout cell improvements
  - Transimpedance amplifier integration
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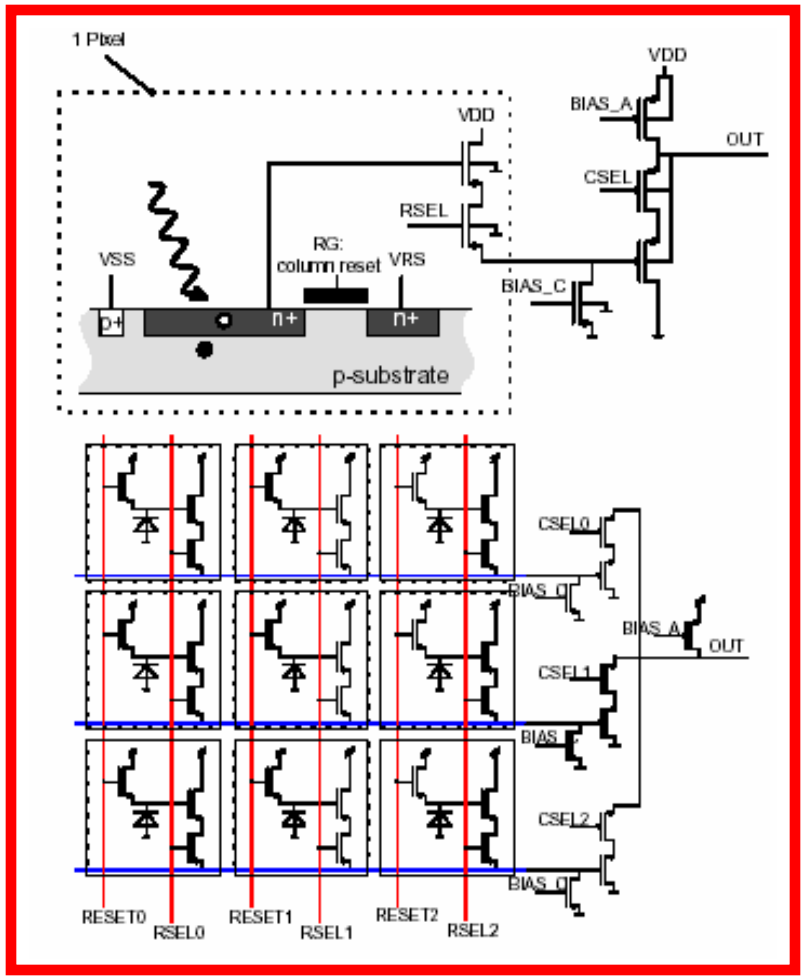
ROIC conventional architecture



Time Domain Multiple Access

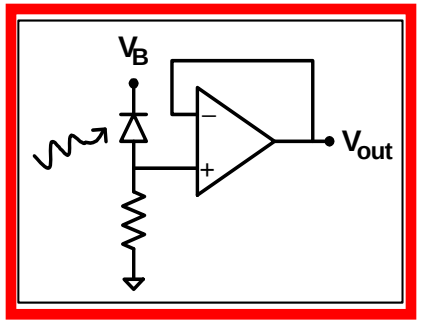
Control signals access every readout cell in a time scheduled manner, sampling the voltage signals and transferring them to the readout bus.

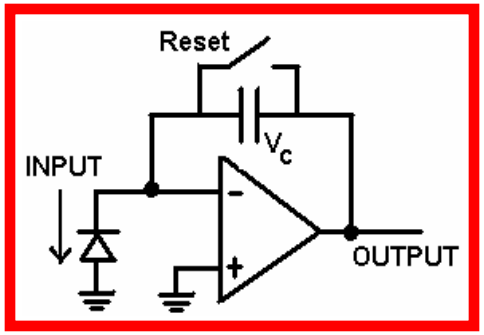
It requires faster electronics for bigger photodetector arrays.

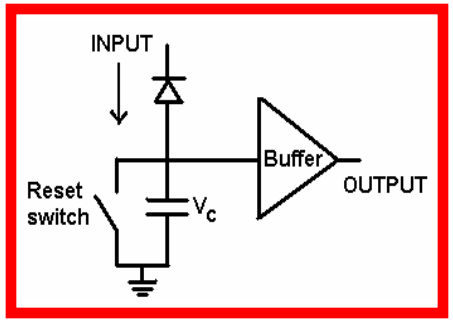
Each readout cell must be capable of storing the required charge, which becomes a problem for big array sizes (1024x1024).

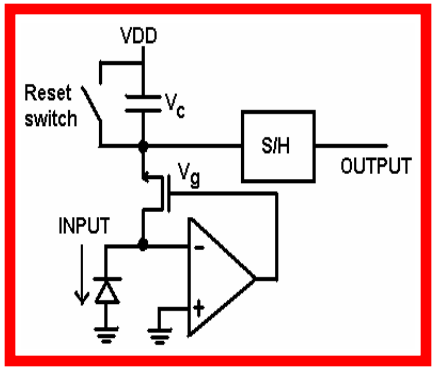
Read Out Cell Architectures

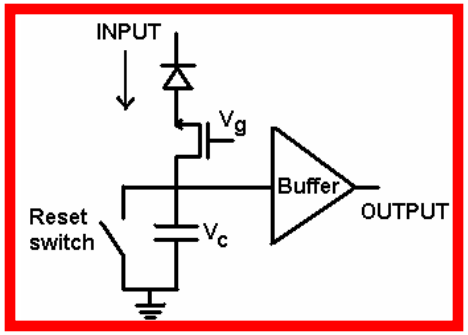
From Direct Injection to Capacitive TransImpedance Amplifier



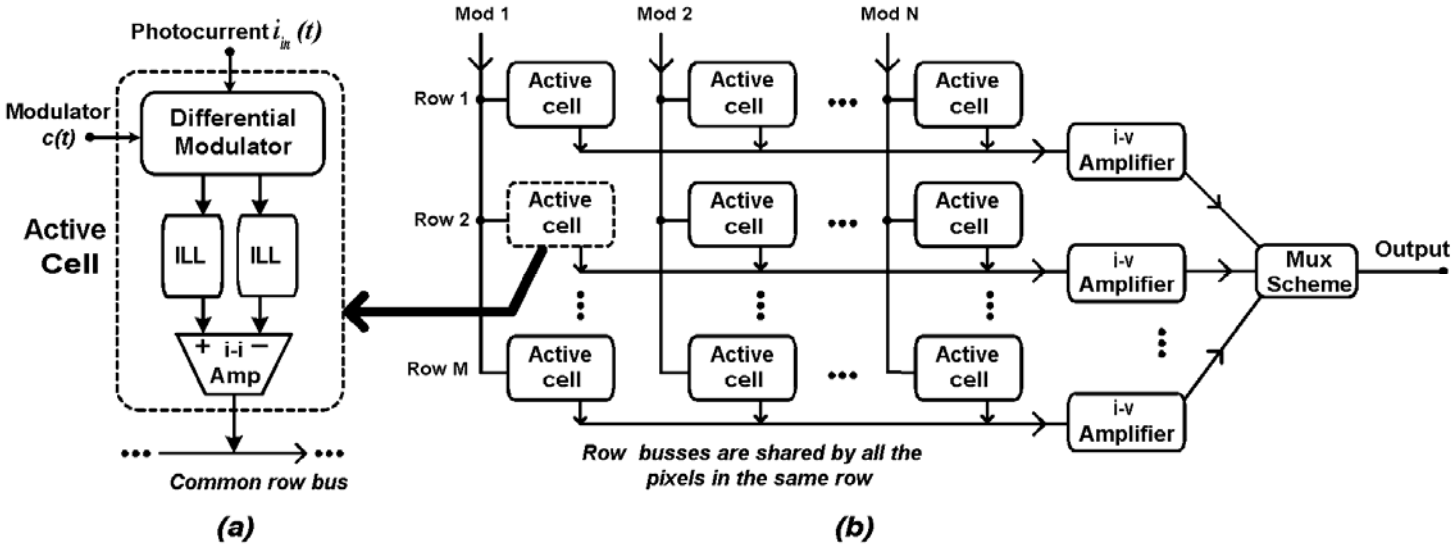








ROIC proposed architecture

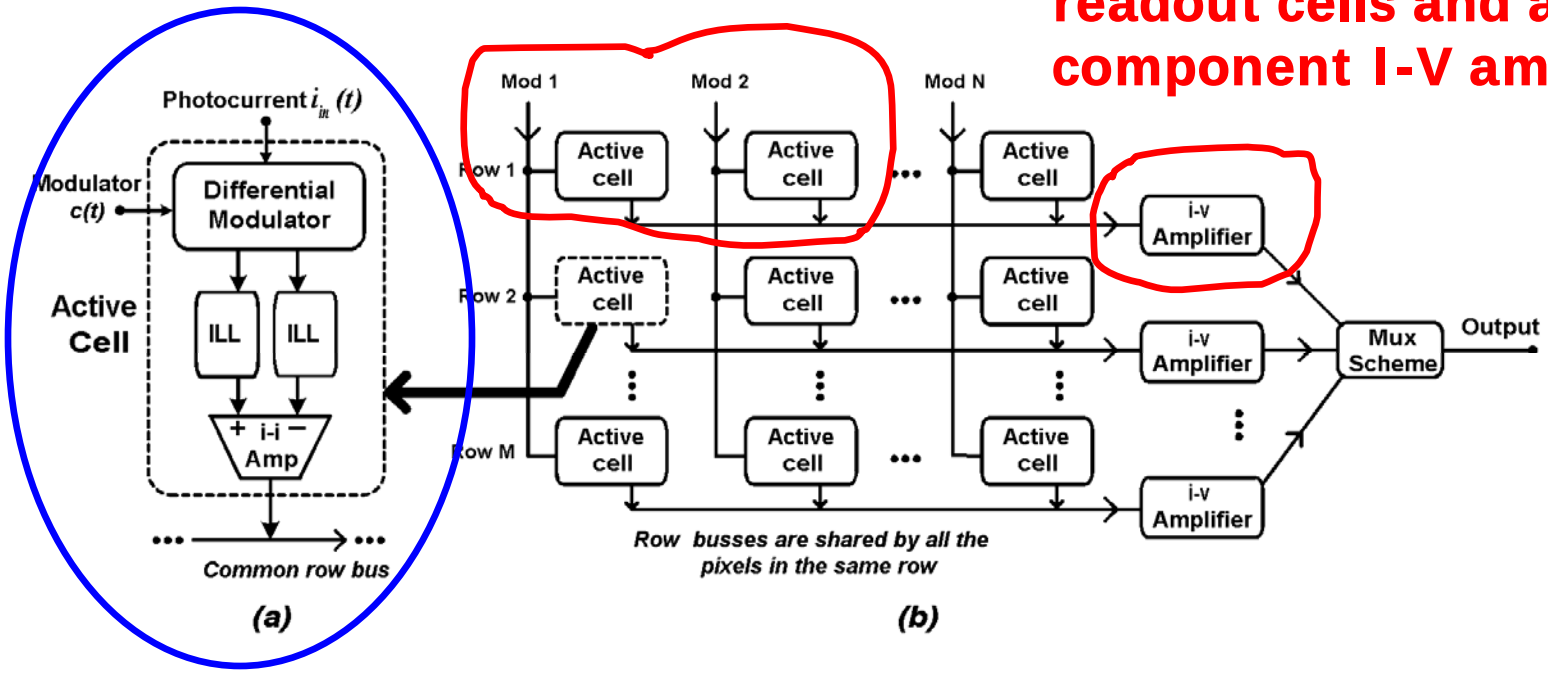


Orthogonal encoding ROIC

- Each column is multiplied by a unique code, and the multiplied signals are summed in the row common bus
- Codes are chosen to minimize cross talk
- Current-to-voltage amplifier per row
- Multiplexer scheme to generate single data stream

Orthogonal Encoding ROIC First Phase Design Tasks

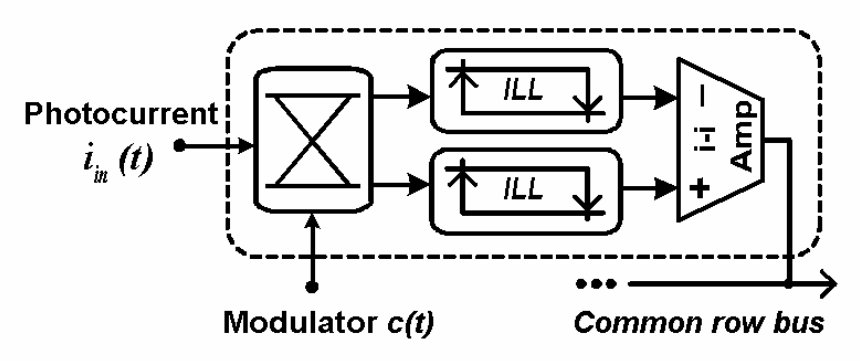
Test system with four readout cells and a discrete component I-V amplifier



Design of the Active Readout Cell

To design and fabricate a test chip for a proof of principle of the active 2D readout technique.

Active Readout Cell: Design Requirements



Readout cell for orthogonal encoding

Multiplies the input current by the code

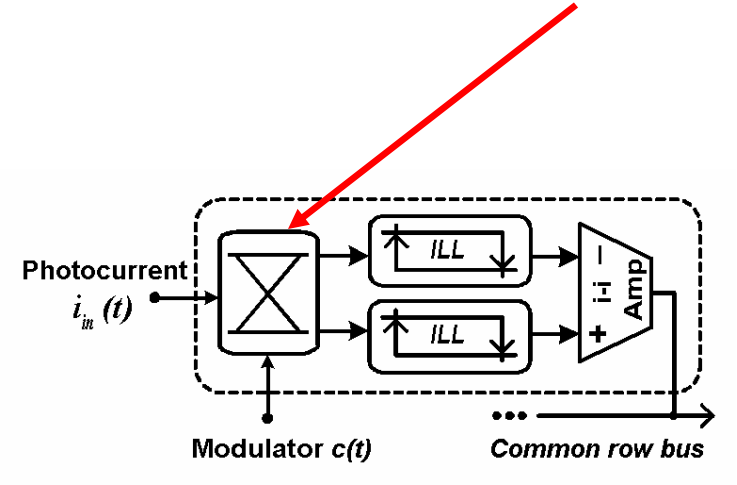
Provides detector virtual ground

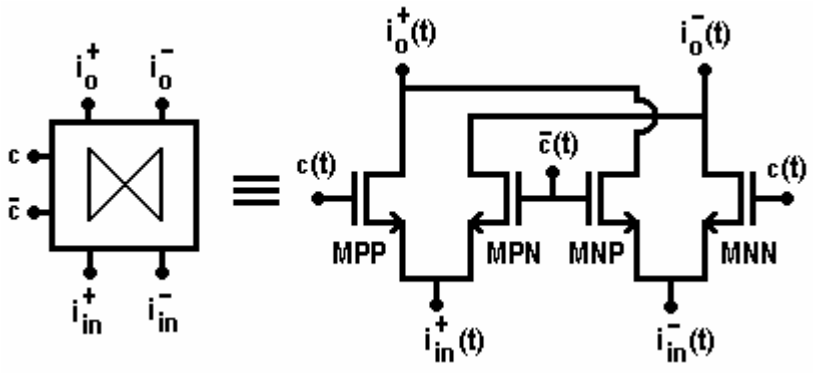
Couples the detector impedance to the bus

Reduces charge injection noise

Active Readout Cell: Implementation

Differential code multiplier





Readout cell for orthogonal encoding

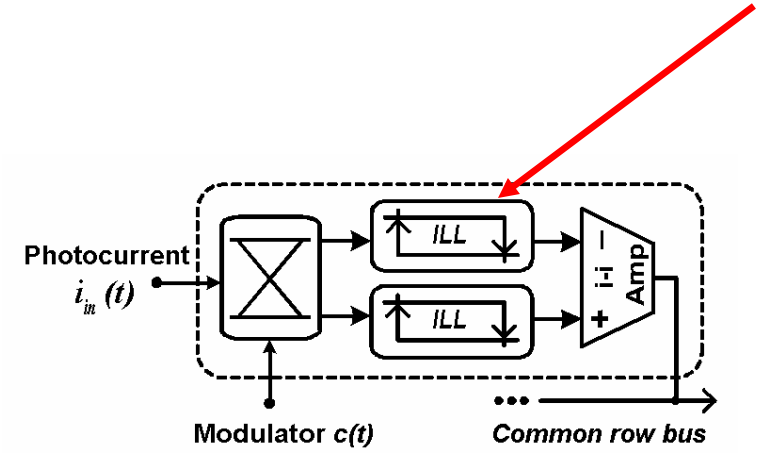
$$i_o^+(t) = i_{in}^+(t)\cdot c(t) + n_c + i_{in}^-(t)\cdot \overline{c}(t) + n_{\overline{c}},$$

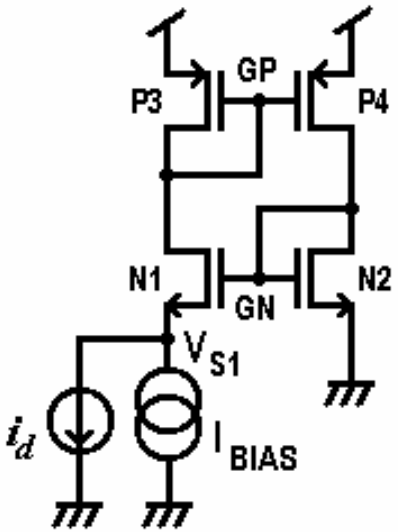
$$i_o^-(t) = i_{in}^+(t)\cdot \overline{c}(t) + n_{\overline{c}} + i_{in}^-(t)\cdot c(t) + n_c,$$

Differential output current $i_{od}(t) = i_o^+(t) - i_o^-(t) = [i_{in}^+(t) - i_{in}^-(t)]\cdot[c(t) - \overline{c}(t)],$

Active Readout Cell

Current Locked Loop ILL





Characteristics

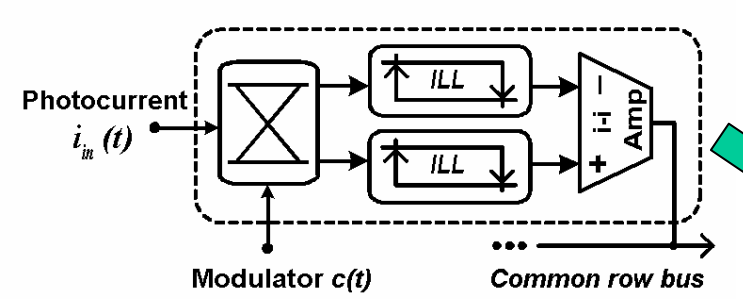
Detector virtual ground

$$\left.\frac{v_{g1}}{v_{s1}}\right|_{low\ freq.} = \frac{-g_1 g_4}{g_2 g_3 - g_1 g_4} = \frac{-\gamma}{1-\gamma}, \text{ with } \gamma = \frac{g_1 g_4}{g_2 g_3}$$

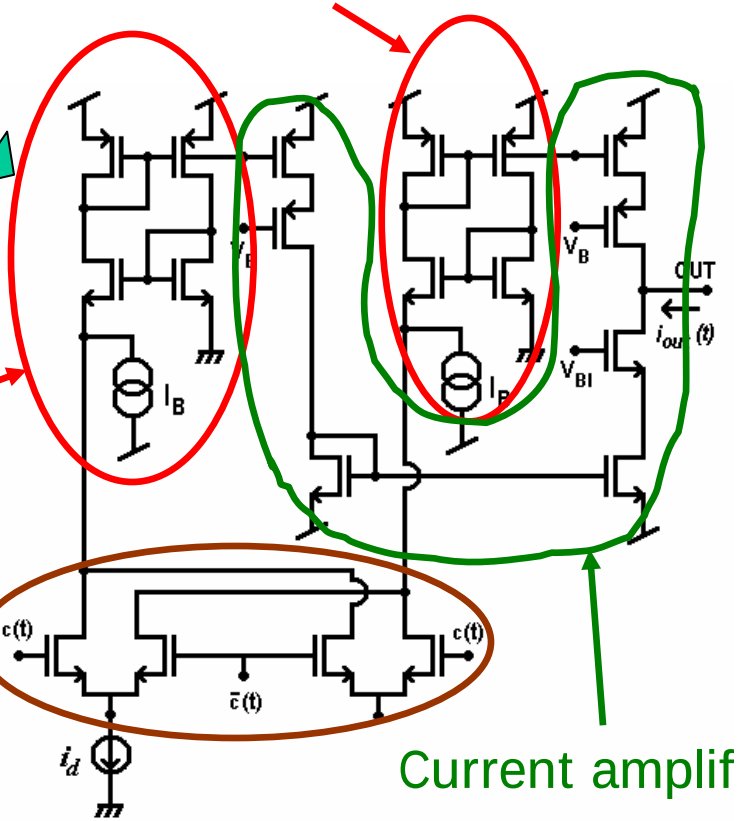
Low input impedance

$$\left.Z_{in}\right|_{low\ freq.} = \frac{1}{g_1}(1-\gamma)$$

Active Readout Cell



ILL Replica



Current Locked Loop (ILL)

- Detector virtual ground
- Low input impedance

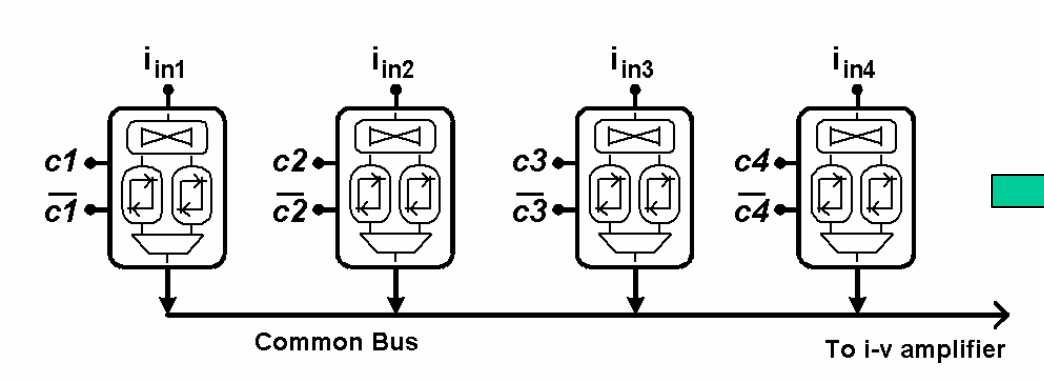
Differential code multiplier

- Signal-code modulation
- Balanced charge injection

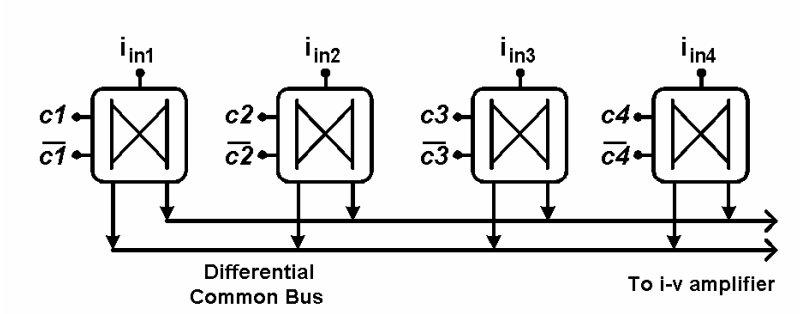
Current amplifier

- Current gain
- High output impedance
- Charge cancellation

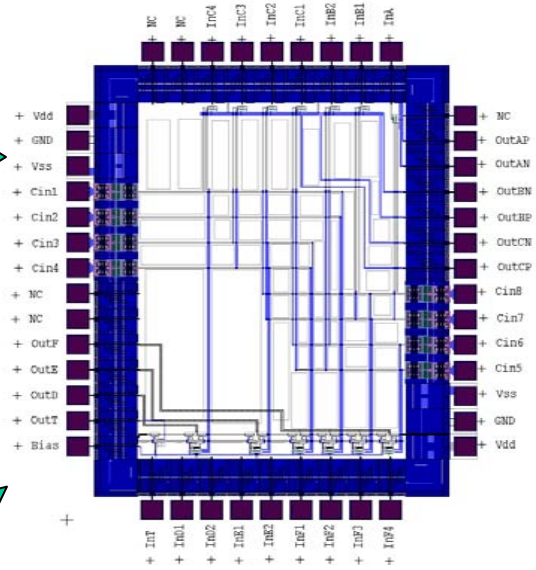
Test chip implementation



4 instances of active readout cell



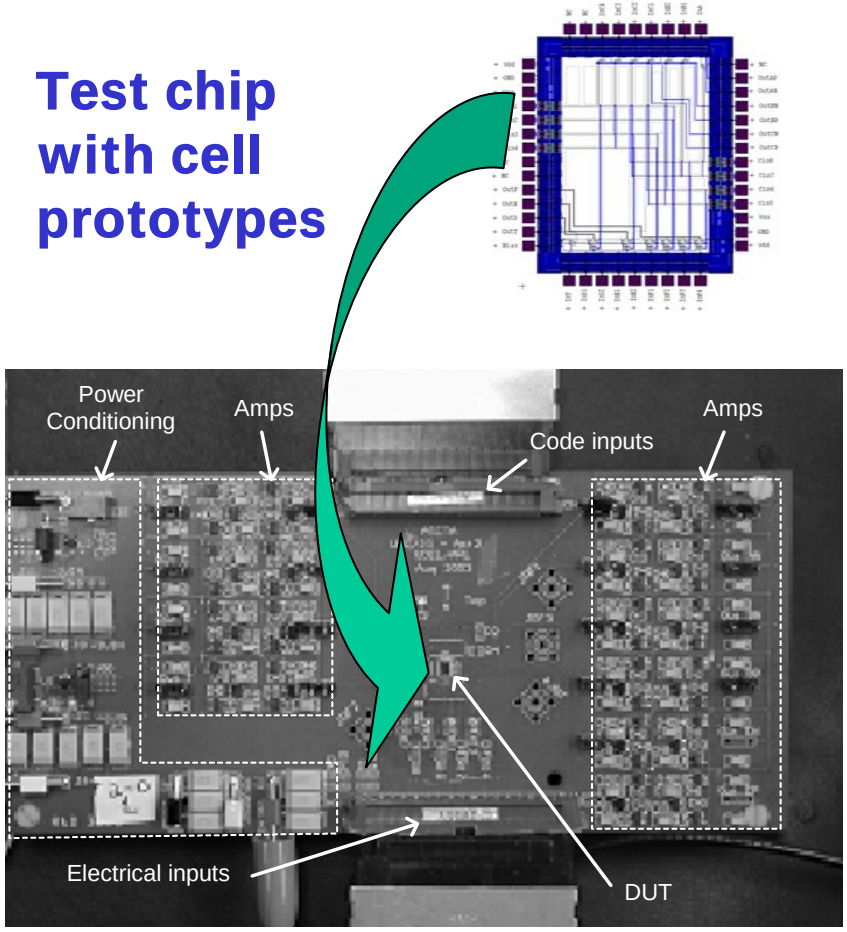
4 instances of cell with input modulator only



Test chip with cell prototypes

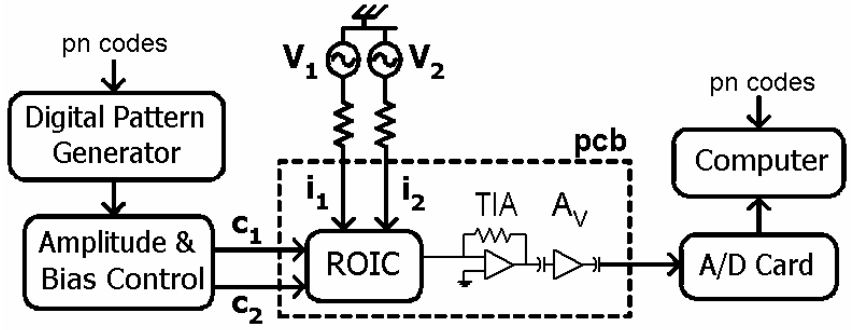
Prototype system testing

Test chip with cell prototypes



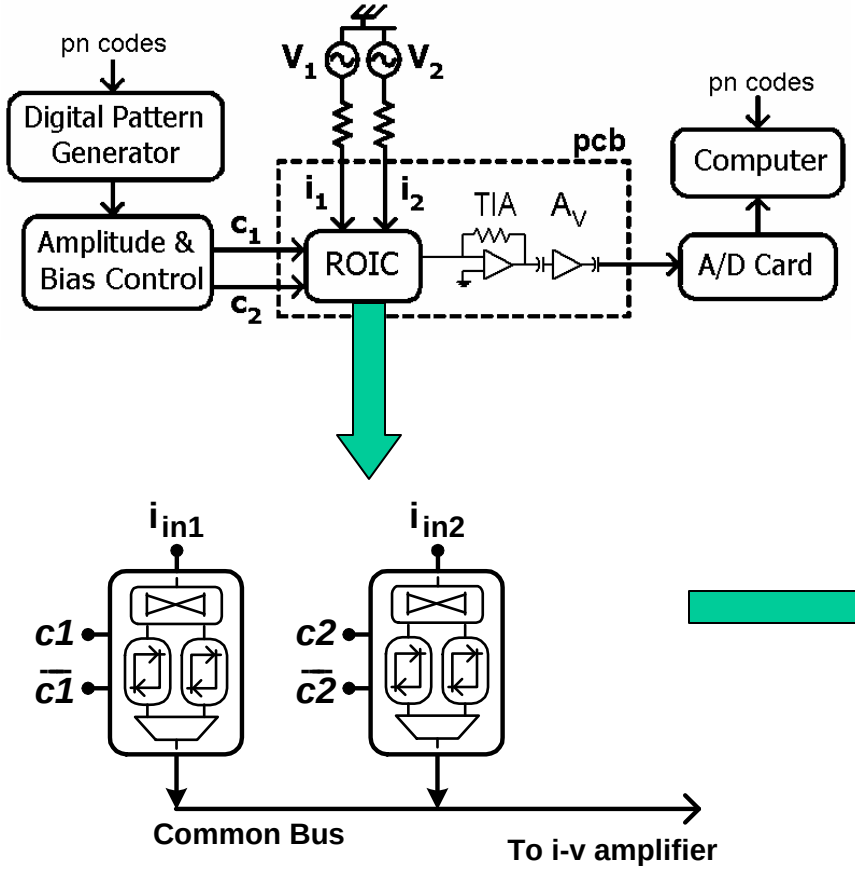
Custom printed circuit board for electro-optical testing

ROIC electrical verification set up

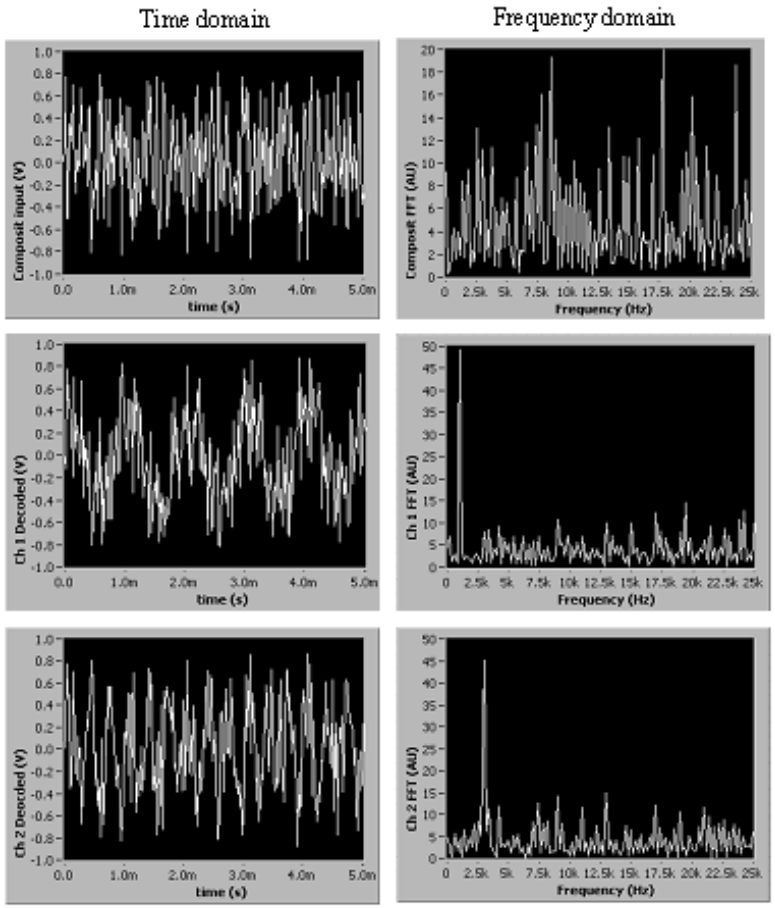


- Code signals generated and conditioned externally
- Voltage sources + Resistors emulate electrical current inputs
- High-gain off-chip transimpedance amplifiers on the pcb
- Data is acquired and processed in the computer

Verification Results



Proof of principle system with 2 encoding cells



Test results

Prototyping phase conclusion

Satisfactory results with the 2 encoding cells experiment confirm validity of the orthogonal encoding scheme for readout circuits

Applicability extends to passive imaging systems

Depending on the system conditions, the orthogonal encoding architecture is advantageous with respect to the conventional time-multiplexed scheme

Integrating the transimpedance amplifiers with improved versions of readout cells should enhance noise performance of the overall system

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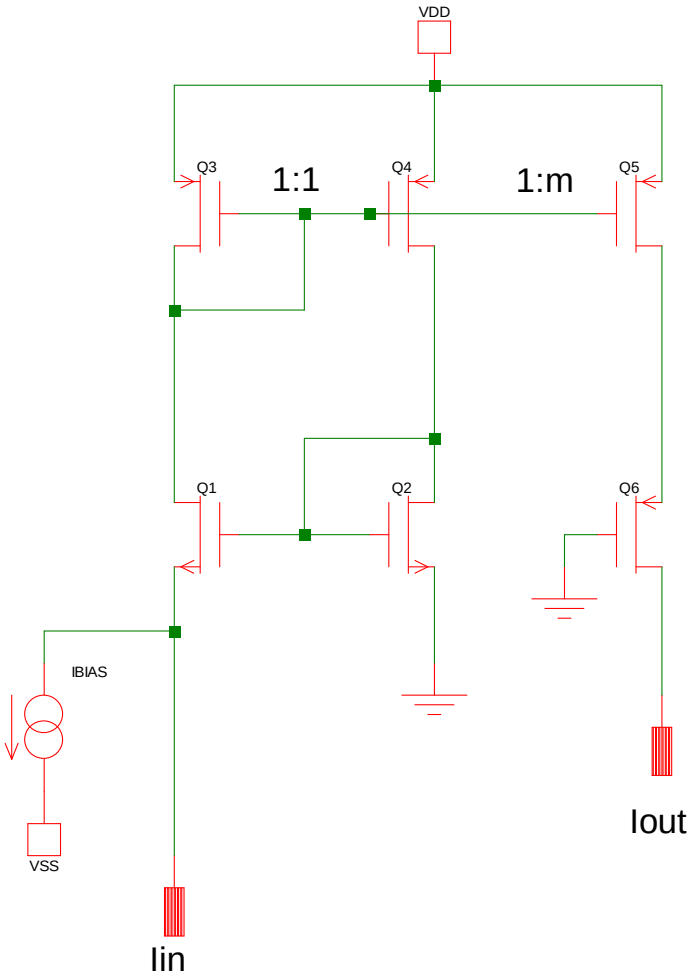
Active Readout Cell Improvements

ILL current gain and noise performance



$$\overline{i_{Q3}^2} = 4kT\gamma g_3$$

$$\overline{i_{out}^2} = 4kT\gamma g_5\left(1+\frac{g_5}{g_3}\right) = 4kT\gamma g_3 m(1+m)$$

Input referred noise

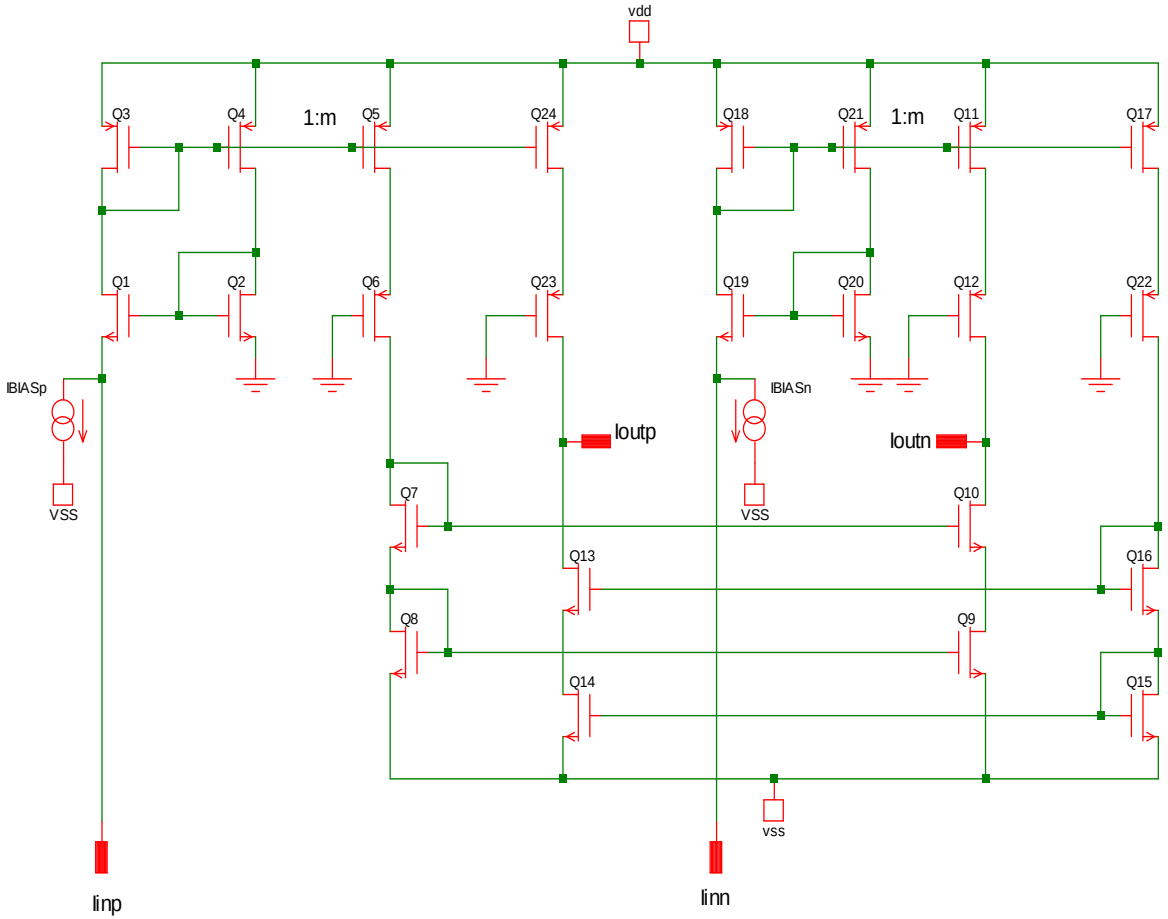
$$\overline{i_{ieq}^2} = \frac{\overline{i_{out}^2}}{m^2} = 4kT\gamma g_3 \frac{(1+m)}{m}.$$

Minimize g_3

Maximize current gain m

Active Readout Cell Improvements

Fully differential architecture



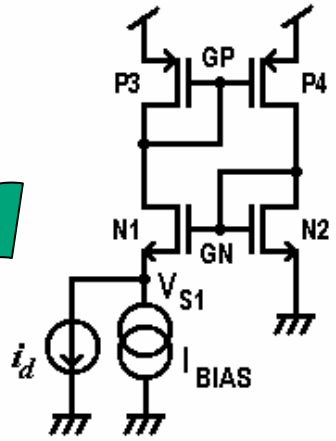
Additional current mirror for complementary output

Improved charge injection cancellation and offset

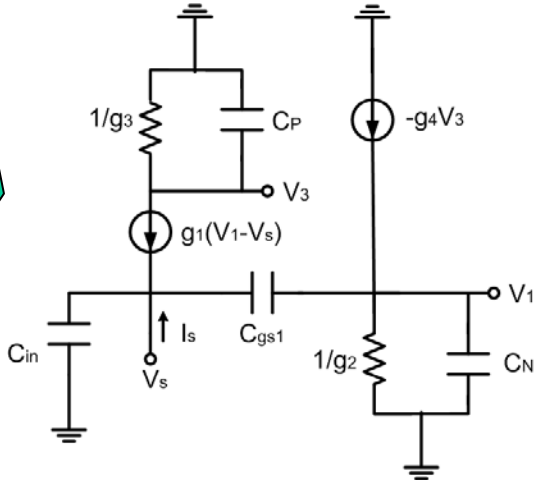
Noise from cascode mirrors is minimized

Active Readout Cell Improvements

Input impedance engineering



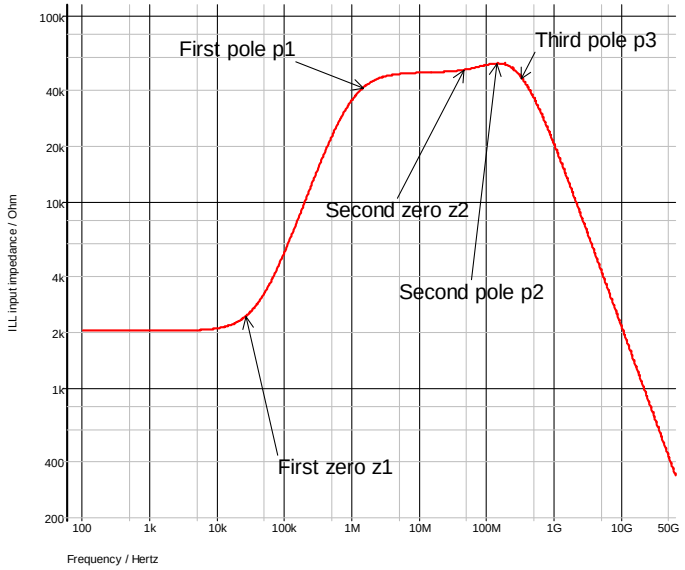
Small-signal model



From small-signal model, solve for Z_{in}

$$Z_{in} = \frac{V_s(s)}{I_s(s)} = \left(\frac{1}{sC_{in}}\right) // \frac{(g_3 + sC_P)(g_2 + s(C_{gs1} + C_N)) - g_1 g_4}{(g_1 + sC_{gs1})(g_3 + sC_P)(g_2 + sC_N)}$$

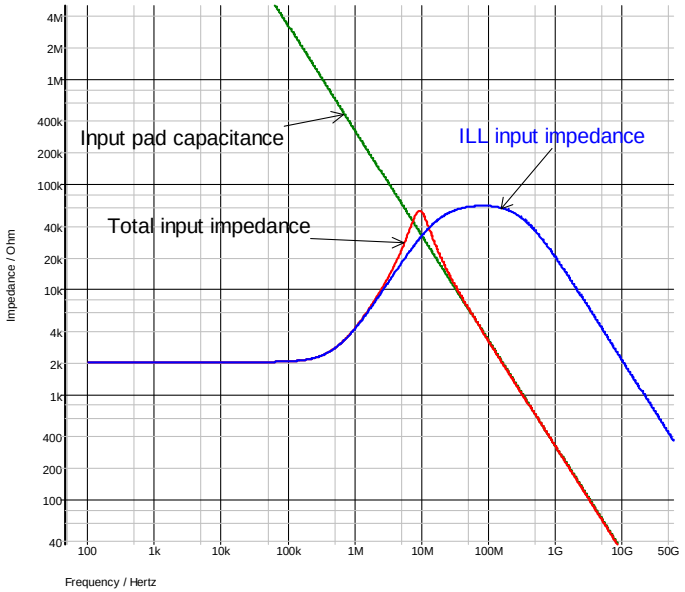
Input impedance without C_{in}



Active Readout Cell Improvements

Input impedance engineering (cont'd)

Input impedance with C_{in}



ILL pole-zero analysis

$$z_1 = \frac{K_z - C_{gs1}g_3 - C_N g_3 - C_P g_2}{2C_P(C_{gs1} + C_N)}$$

$$z_2 = \frac{-K_z - C_{gs1}g_3 - C_N g_3 - C_P g_2}{2C_P(C_{gs1} + C_N)}$$

$$p_1 = -\frac{g_3}{C_P}$$

$$p_2 = -\frac{g_2}{C_N}$$

$$p_3 = -\frac{g_1}{C_{gs1}}$$

$$K_z = \sqrt{C_{gs1}^2 g_3^2 + 2C_{gs1}(C_N g_3^2 + C_P(2g_1g_4 - g_2g_3)) + C_N^2 g_3^2 + 2C_N C_P(2g_1g_4 - g_2g_3) + C_P^2 g_2^2}$$

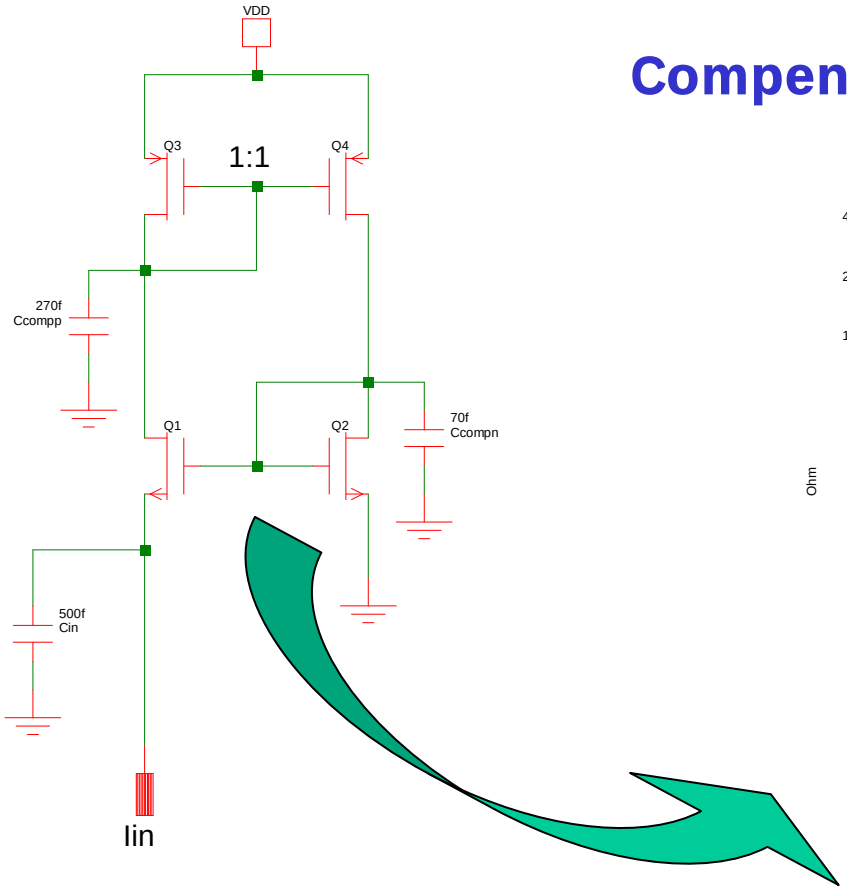
C_P controls p_1 and z_1, but also moves z_2 to the left

C_N moves p_2 close to z_2, canceling its effect

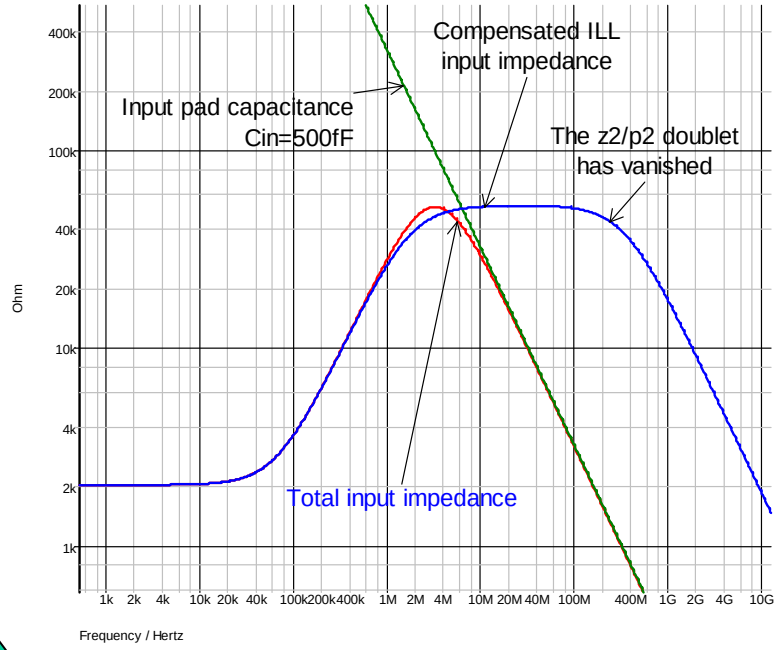
p_3 determines overall gain-bandwidth

Active Readout Cell Improvements

Input impedance engineering (cont'd)



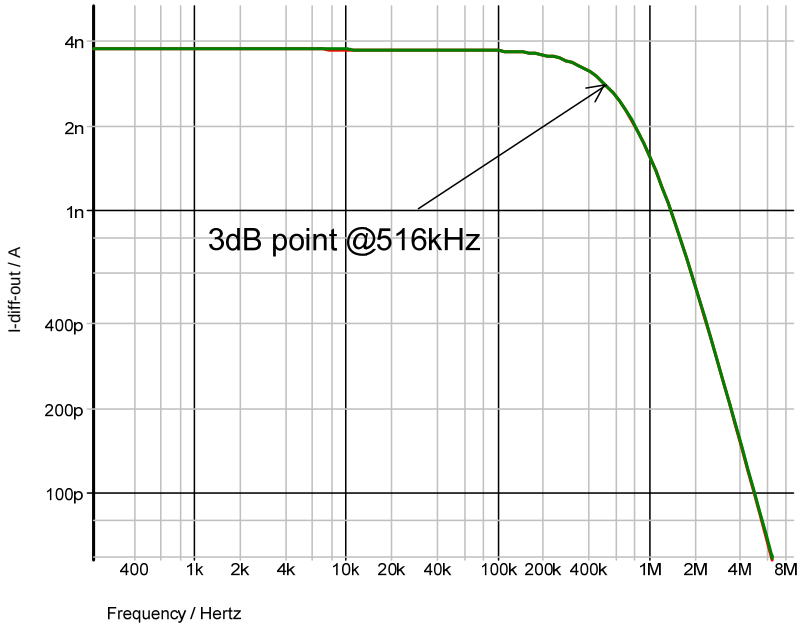
Compensated input impedance with C_{in}



C_P = 270fF and C_N = 70fF compensate the input impedance for C_{in} = 500fF

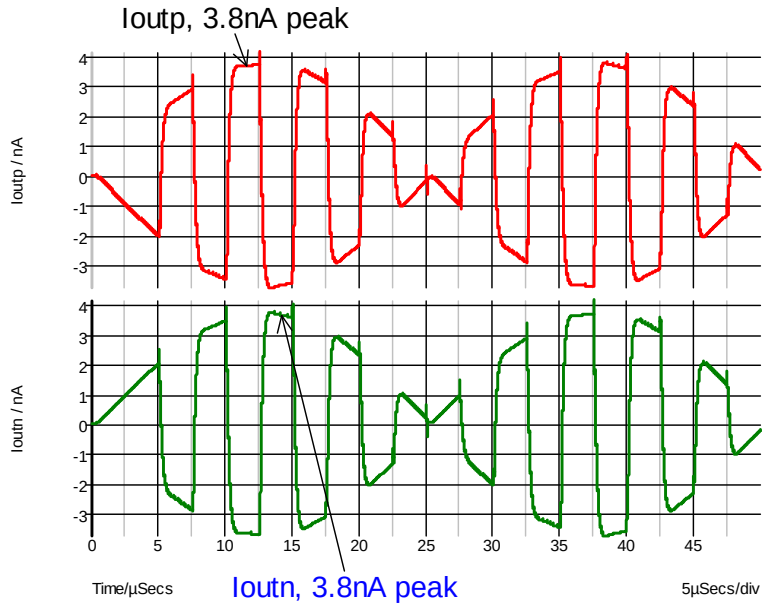
Improved Active Readout Cell Performance

Frequency response



Designed for 500kHz code bandwidth (16 cells)

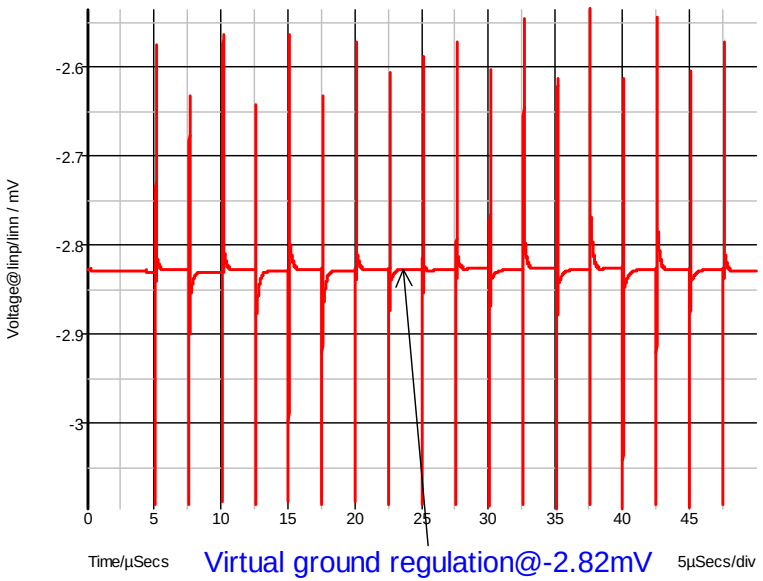
Transient response



Current gain of 3.8A/A

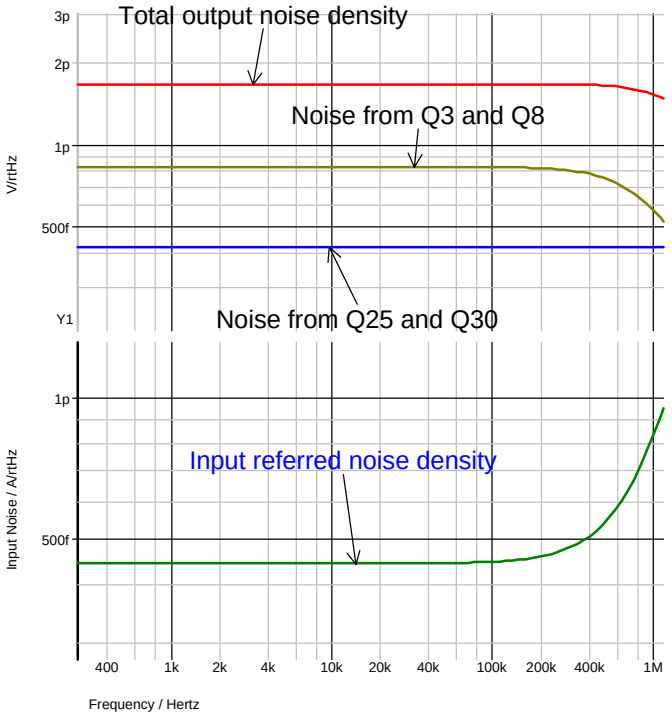
Improved Active Readout Cell Performance

Virtual ground regulation



Between -3.1mV and -2.6mV

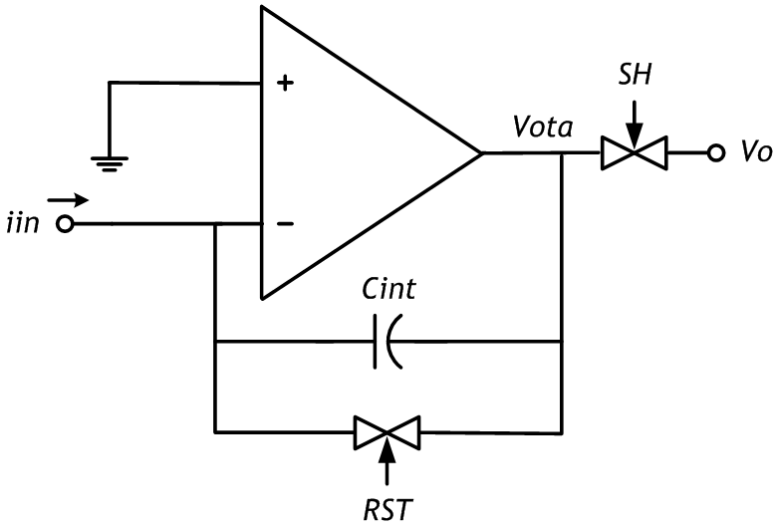
Noise performance



Input referred noise 400fA/rtHz

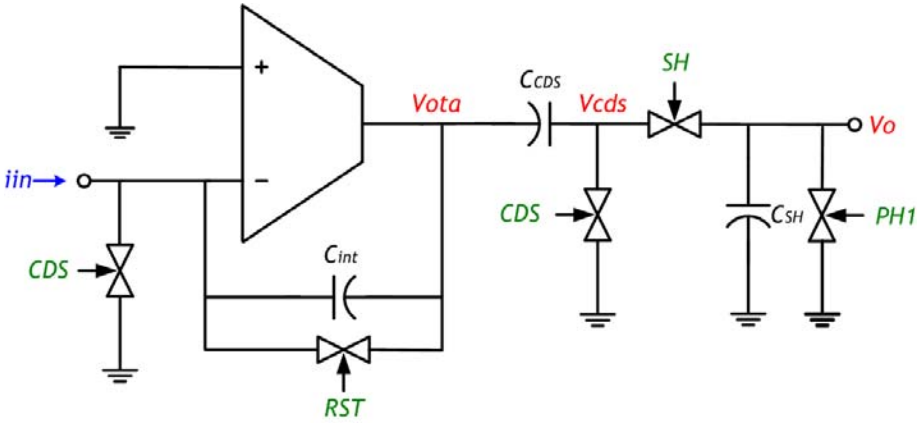
Transimpedance amplifier implementation

Capacitive TIA (CTIA)



RST switch injects charge and produces sampling (kT/C) noise

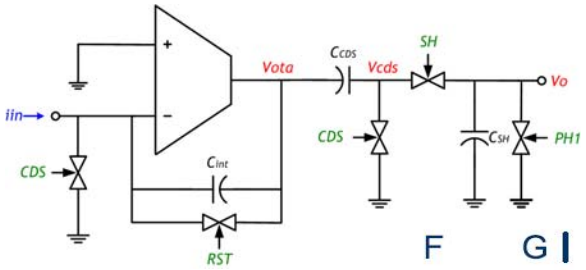
CTIA with correlated double sampling (cds)



CDS structure removes sampling noise

SH capacitor produces voltage divider

CTIA system-level implementation



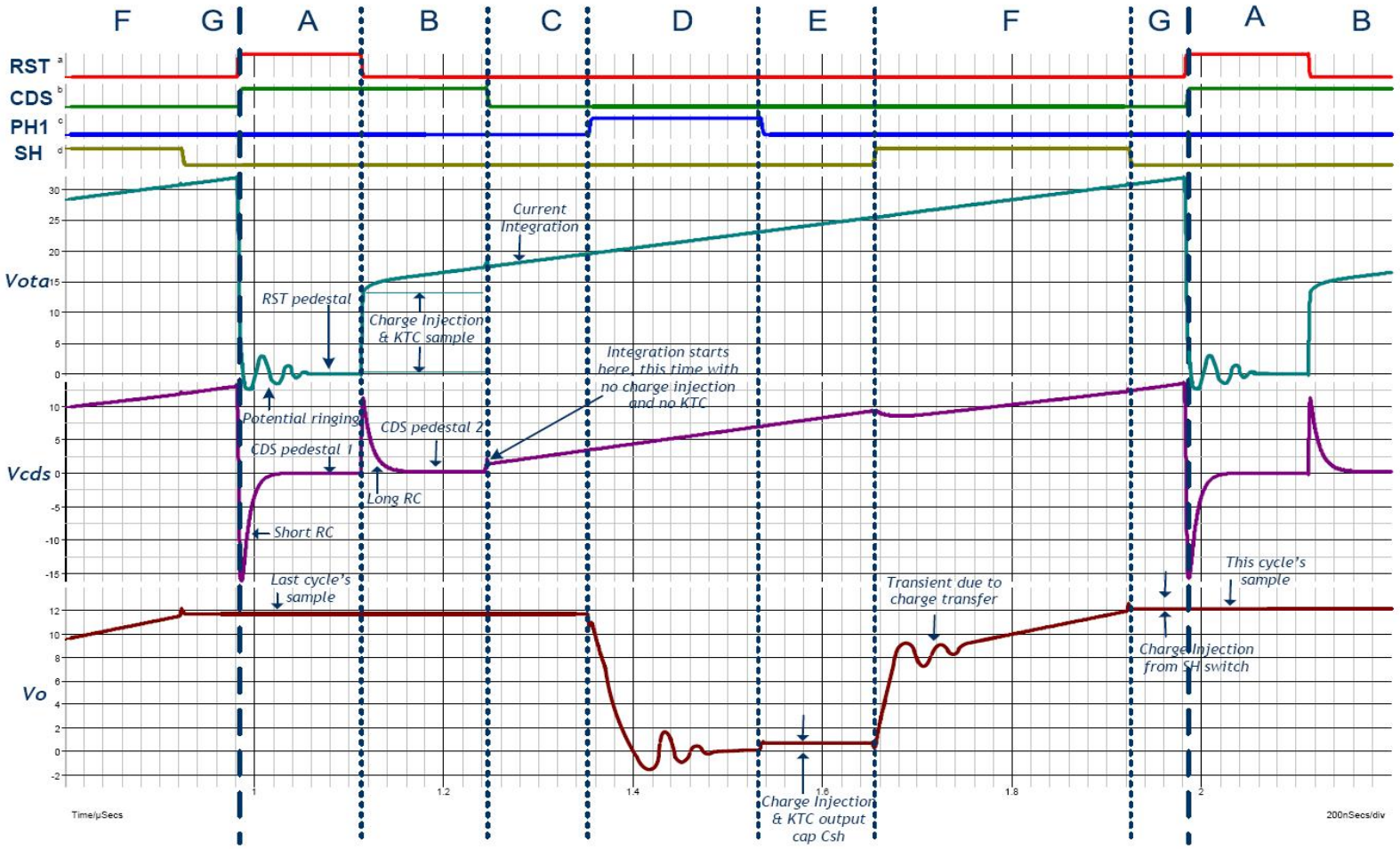
Dynamics of CTIA system with cds

Control signals

OTA output

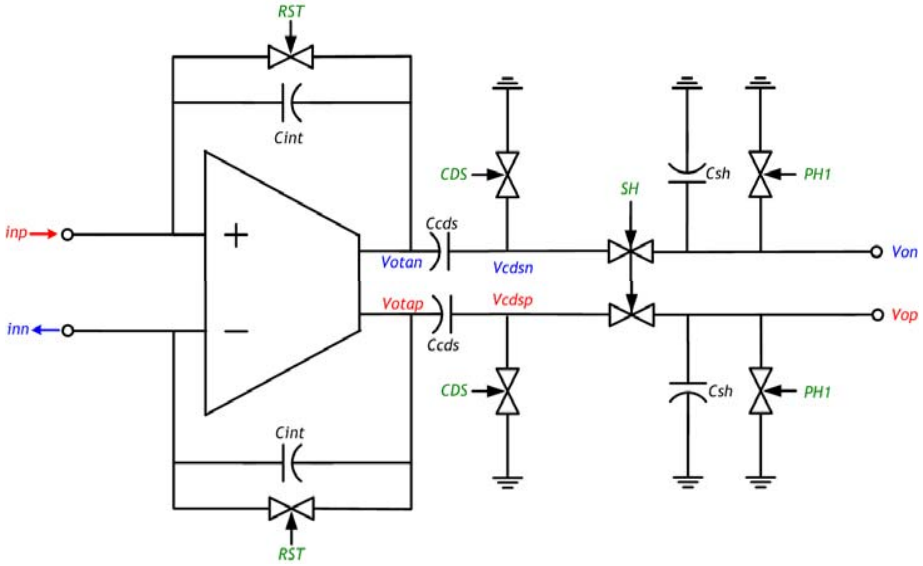
cds output

System output

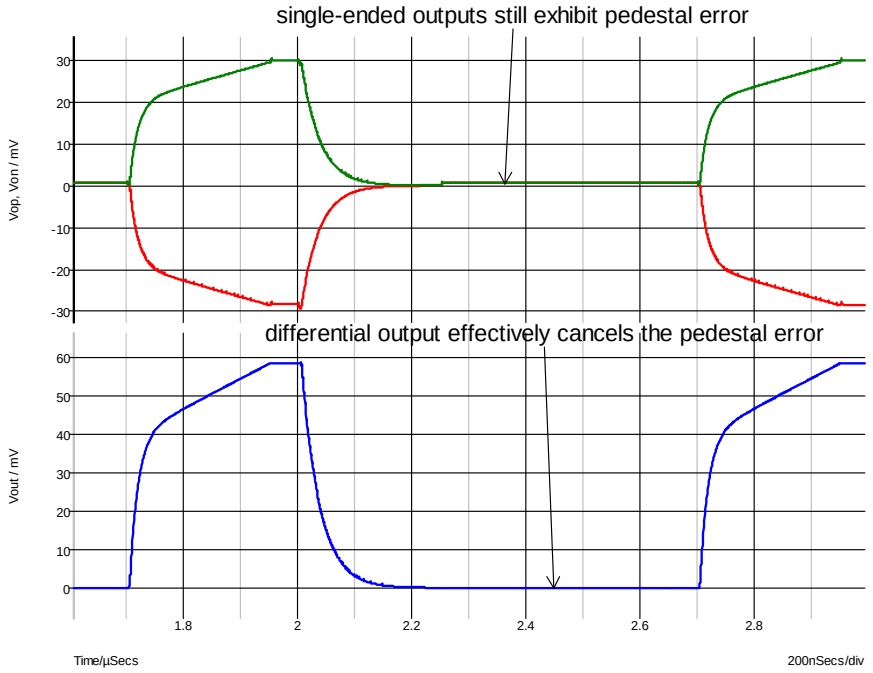


CTIA system-level implementation

Advantages of fully differential CTIA system



Fully differential CTIA system

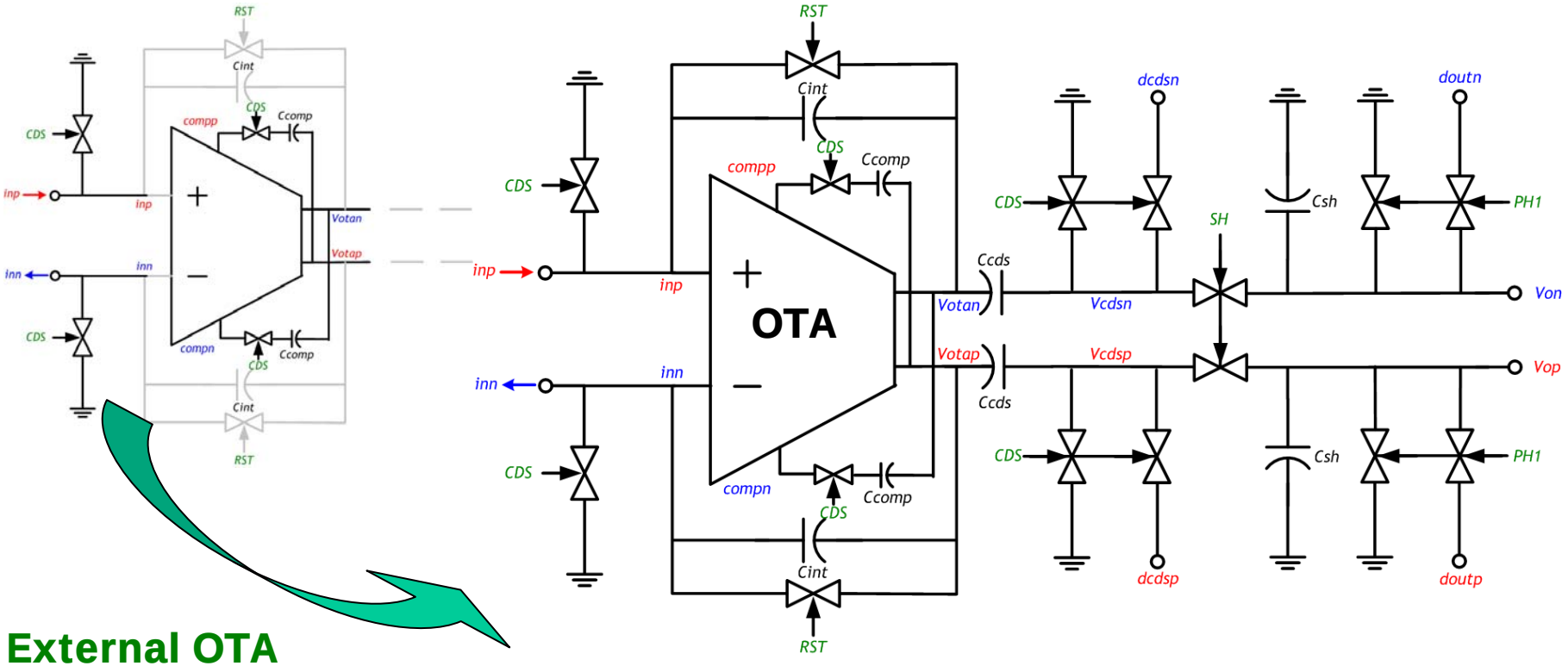


Transient response of

Single-ended vs. Differential output

CTIA system-level implementation

External OTA compensation and sizing of switches and capacitors



External OTA compensation

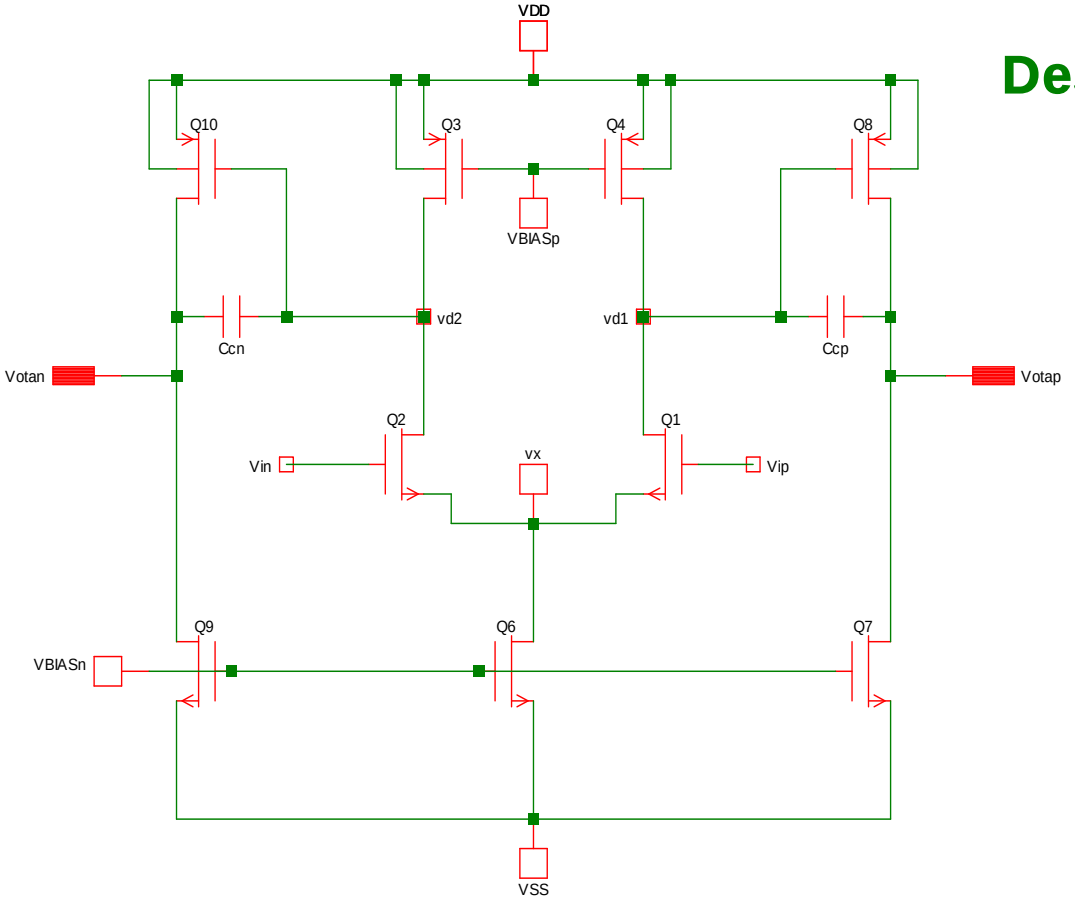
Input stabilization switches

C_{CDS} = 5pF, C_{SH} = 1pF, C_{comp} = 3pF, C_{int} = 50fF

Switches designed for worst-case scenario R_{SW} ~ 1kΩ

OTA circuit-level implementation

2-stage Miller compensated OTA, design requirements



Design requirements

- Gm > 250mSie
- a_{vo} (2% settling accuracy) > 40k
- Input referred noise < 5nV/rtHz
- Dominant pole and non-dominant pole more than three decades apart
- Output common-mode < 10mV
- CMRR > 60dB
- Input differential capacitance not to exceed 15pF
- Output swing of 2.4Vpk-pk
- Dual power supplies of ±2.5V
- Best effort on power consumption and layout area

OTA design methodology

FIRST PHASE OF DESIGN: FROM SPECS TO CIRCUIT PARAMETERS

Specifications		
Settling accuracy:= E	2.00%	
Settling time:= ts	5.00E-08	sec
Dynamic Range:= DR(dB)	40.00	dB
Closed Loop Gain:= c		V/V
Vin step:= Vstep		V
Supplies:= VDD= -VSS	2.50	V

Initial design knobs		
C feedback (Cf)	2.00E-14	F
C series (Cs)		F
C input (Cp) (assumed)	1.50E-11	F
CCDS (CDS cap)	5.00E-12	F
CSH (SH cap)	1.00E-12	F
Delta Vod (Vpk-pk)'	3.00	V
Static error%:= St.err%	0.80	

Preliminary calculations		
F = Cf / (Cf+Cp)	1.33E-03	V/V
Ao ~ 1 / F	7.51E+02	V/V

Constants		
Boltzmann	1.38E-23	$#%
Temperature	300	K
q	1.60E-19	C

Transitor parameters	NMOS	PMOS	
Cox	2.46E-15	2.38E-15	F/um^2
Col_factor	2.01E-16	2.61E-16	F/um
uCox	1.14E-04	3.78E-05	A/V^2

1. From noise to first stage design

Preliminary calculations		
Co = CCDS//CSH + Cf(1-F) + Cgd7+ Cdb7+ Cdb8	8.53E-13	F
gm3/gm1 = V1*/V3*	3.78E-01	V/V
gm7/gm8 = V8*/V7*	1.43E+00	V/V
Signal Power (Psig): [Vpk/sqrt(2)]^2	1.125	V²
Noise Power Budget (Pnoi): Pnoi = Psig/[10^(DR/10)]	1.13E-04	V²

FIRST STAGE DESIGN From simulations and iteration:		
Gain of first stage *a1*	292	V/V
1st st. transconductance *gm1*	1.42	mSie
R1 = a1 / gm1 (required)	206	kOhm
Diff pair, ro1 (from sims) =	225	kOhm
Load, ro3 (from sims) =	908	kOhm
Diff. pair (N) Vov:= V1*	170	mV
Act. Load (P) Vov:= V3*	450	mV
R1 (achieved) = ro1 // ro3	180	kOhm
and gm3 = gm1. V1* / V3*	0.54	mSie
IBIAS1 = gm1.V1* / 2	120.70	uA
ISS = 2*IBIAS1	241.40	uA

Sizes W = L.gm / (u.Cox.V*)	W(um)	L(um)
M1,M2 (differential pair)	221	3.000
M3,M4 (active load)	126	4.000

Input Noise Power Density due to 1st stage:		
2*(8/3)(KT/gm1)*(1+gm3/gm1)	2.14E-17	V2/Hz
Input Noise Voltage Density due to 1st stage: sqrt(ans)	4.63E-09	V/rtHz

2. Static accuracy implications

Static error:= E_st		
E_st = E * St.err%	1.600%	
a0 (minimum)		
a0 = 1 / (F.E_st)	46.94	k
a0 (dB)	33.43	dB
Gain of second stage, a2 (minimum)		
a2=a0 / a1	160.74	V/V

3. Dynamic Accuracy

Dynamic error:= E_dyn		
E_dyn = E - E_st	0.400%	
Slewing (N/A for CTIA)		
Slew time (t_slew)	0.00E+00	sec
SR_ext = (B-1).IBIAS / Cc		V/us
SR_int = IBIAS / C		V/us
SR_ext = SR_int		
then IBIAS-slew:		
(DeltaVod/2)*C / t_slew		A
B(2nd:1st BIAS ratio) = 1 + Co/C		
Linear		
Linear time:= t_lin = ts-t_slew	5.00E-08	sec
Linear accuracy:= E_lin		
E_lin = E_dyn (NO SLEW)	0.400%	
minimum OTA's transconductance:		
Gm_s = -(Co/F)*[ln(E_lin)/T_li	7.08E-02	Sie
or desired Gm	4.00E-01	Sie
Gm = max(Gm_s, desired Gm	4.00E-01	Sie
Then IBIAS becomes		
max(IBIAS-slew,IBIAS-linear)	241.40	uA

3. From total Gm and a2 to second stage design

Requirements for second stage (minimum)		
a2 (minimum)	160.74	
gm8 = Gm / a1 (minimum)	1.37E-03	Sie
R2 = a2 / gm8 (minimum)	1.17E+05	Ohm

SECOND STAGE DESIGN From simulations and iteration:		
Gain of second stage *a2*	150	V/V
2nd st. transconduct.*gm8*	3.60E-04	Sie
R2 = a2 / gm8 (required)	4.17E+05	
Com. src. ro8 (from sims) =	1.48E+05	
Load CS, ro7 (from sims) =	2.89E+05	
Com src. (P) Vov:= V8* (from sims)	4.45E-01	V
Load CS (N) Vov:= V7* (from sims)	3.11E-01	V
R2 (achieved) = ro7 // ro8	9.79E+04	
and gm7 = gm8. V8* / V7*	5.15E-04	
IBIAS2 (in paper) = gm8.V8* / 2	3.05E-04	A
IBIAS2 (from sims)	2.50E-04	

Sizes W = L.gm / (u.Cox.V*)	W(um)	L
M8,M10 (common source)	8.56E+01	4.000
M7,M9 (active loads)	7.29E+01	5.000

Input Noise Power Density due to 2nd stage:		
(1/a1)(8/3)(KT/gm8)(1+gm7/gm8)	6.71E-20	V2/Hz

SECOND PHASE OF DESIGN: TRANSISTOR SIZES and VERIFICATION

4. Tweaking in the simulator

Important values so far		
gm1	1.42	mSie
R1	205.63	kOhm
gm8	0.36	mSie
R2	97.88	kOhm

Initial transistor sizes	W(um)	L(um)
M1,M2 (differential pair)	221	3.0
M3,M4 (active load)	126	4.0
M8 (common source)	86	4.0
M7 (2nd stage bias)	73	5.0

Sizes after tweaking in sim	W	L
M1,M2 (differential pair)	200	3.000
M3,M4 (active load)	100	4.000
M8 (common source)	100	4.000
M7 (2nd stage bias)	80	5.000
and for CMFB amplifier (from sims)		
M14,M14a,M15,M15a (diff pa	10	0.800
M16, M17 (act. Load)	80	5.000
M18 (diff pair bias)	100	4.000

5. LAYOUT sizes

Sizes for LAYOUT fingers (M=16)	Wn	L
M1,M2 (differential pair)	12.425	2.975
M3,M4 (active load)	6.3	4.025
M8 (common source)	6.3	4.025
M7 (2nd stage bias)	5.075	5.075
and for CMFB amplifier (from sims)		
M14, M14a, M15, M15a (8 fingers)	1.225	0.875
M16, M17 (act. Load)	5.075	5.075
M18 (diff pair bias)	6.3	4.025

Yielding transistor sizes of	W	L
M1,M2 (differential pair)	198.8	2.975
M3,M4 (active load)	100.8	4.025
M8 (common source)	100.8	4.025
M7 (2nd stage bias)	81.2	5.075
and for CMFB amplifier		
M14, M14a, M15, M15a (diff pair)	9.8	0.875
M16, M17 (act. Load)	81.2	5.075
M18 (diff pair bias)	100.8	4.025

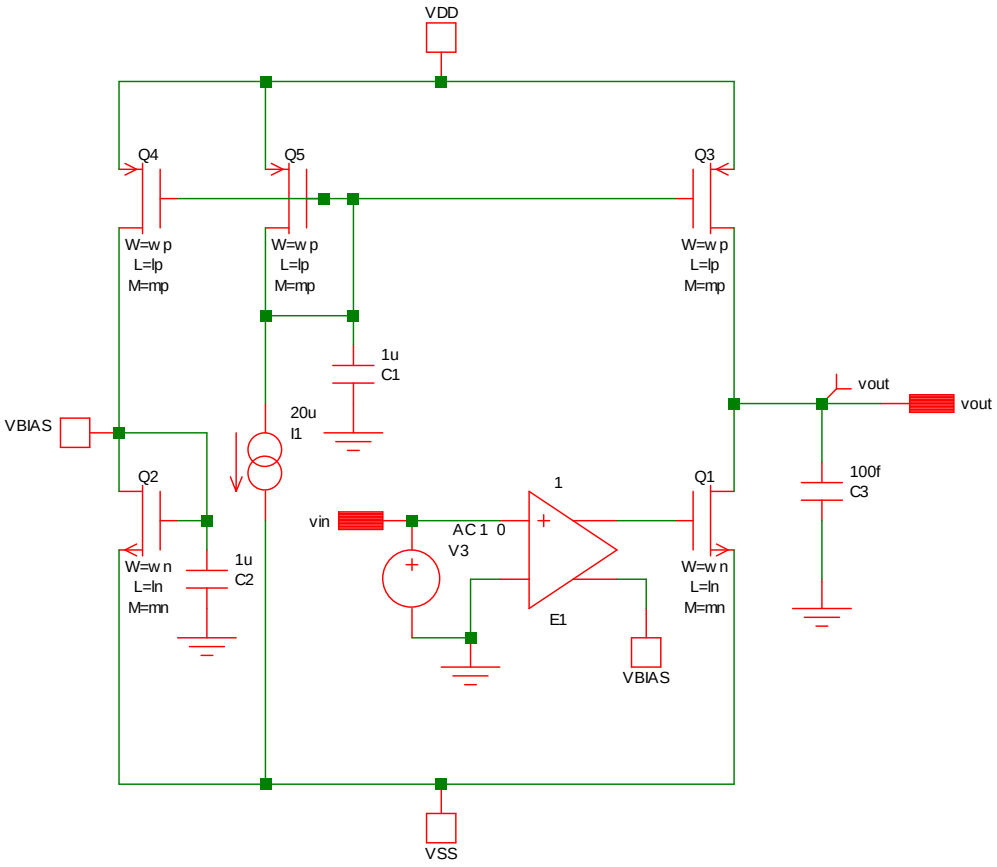
6. Rough verification

Col = Col_factor.W		
Cgs = (2/3)W.L.Cox + Col		
Cgd = Col		
Cgs1,2	1.02E-12	F
Cgd1,2	4.02E-14	F
Cgs8	6.61E-13	F
Cgd8	2.61E-14	F
Compensation cap C	1.00E-15	F
Check for consistency, hopefully Cp-new~Cp		
Cp-new = Cgs1+Cgd1.(1+a1)	1.28E-11	
Frequency response		
fd = 1/ (2.pi.R1.(gm8.R2.(C+Cgd8)+	########	kHz
fnd = gm8/(2.pi.Co)	255.50	MHz
att = 20.log(fnd/fd)		

COLOR CODES	
	SPECS
	KNOBS
	PARTIAL VALS
	FINAL VALUES

OTA design methodology

First and second stage design strategy



Circuit for design of amplification stage

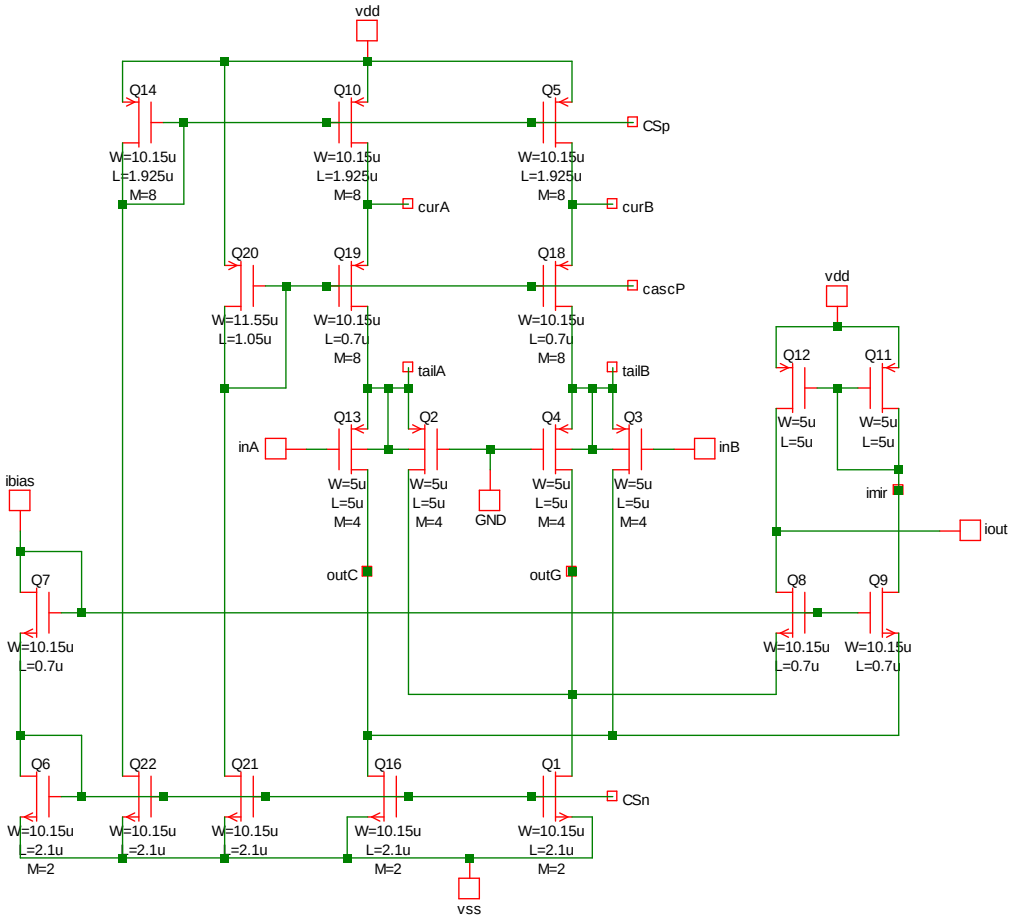
Transistor models from vendor are used to optimize the design of a single stage of amplification with active loading

Bias conditions are replicated, and noise from biasing strategy is properly filtered out

Design results are back-annotated in work sheet

OTA design methodology

Common-Mode amplifier design



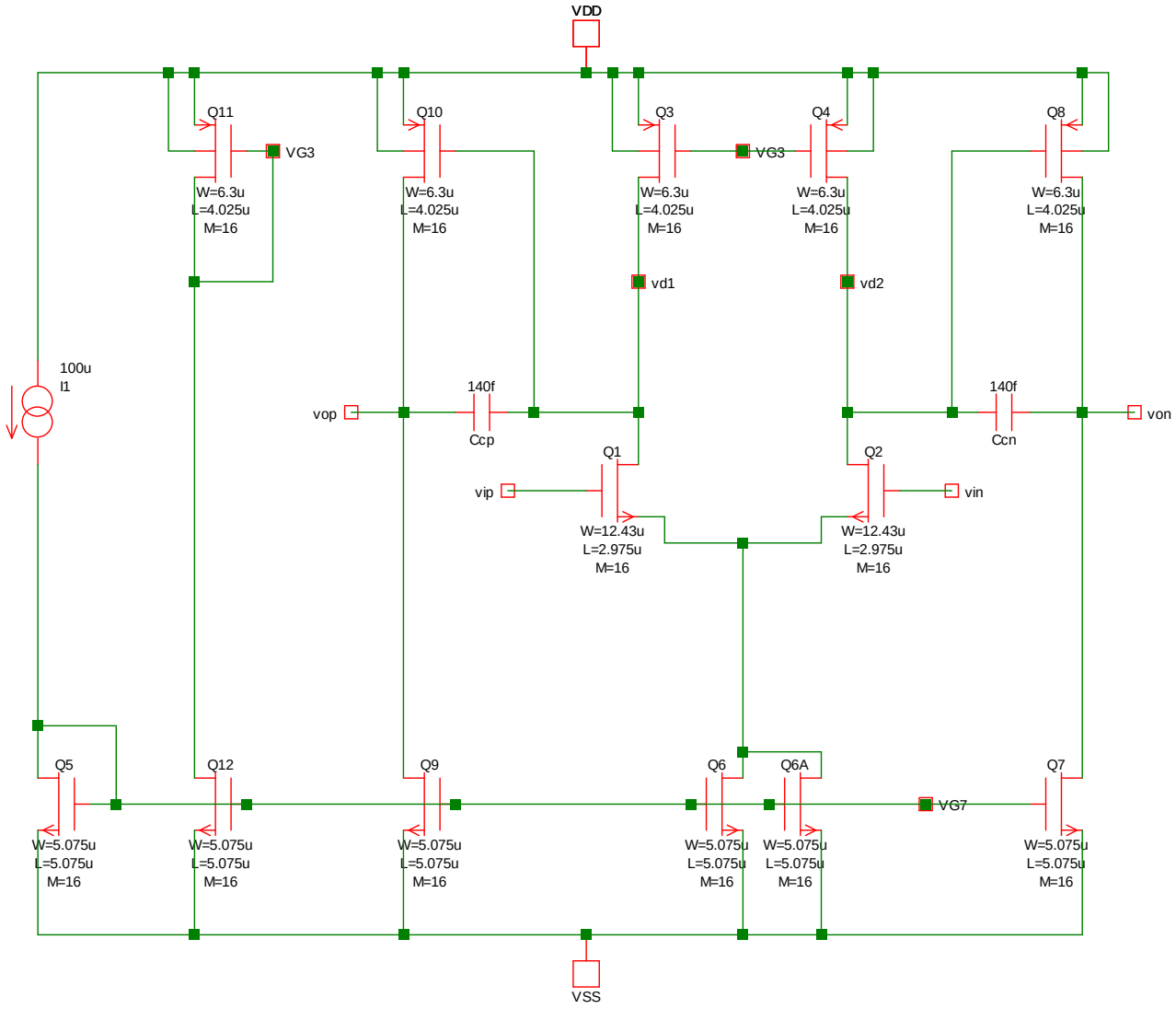
Common-mode amplifier circuit

Q13 and Q3 compute common-mode voltage from the OTA output and “compare” it to the desired value (GND)

The amplifier produces a current output that regulates the common-mode voltage in the differential amplifier

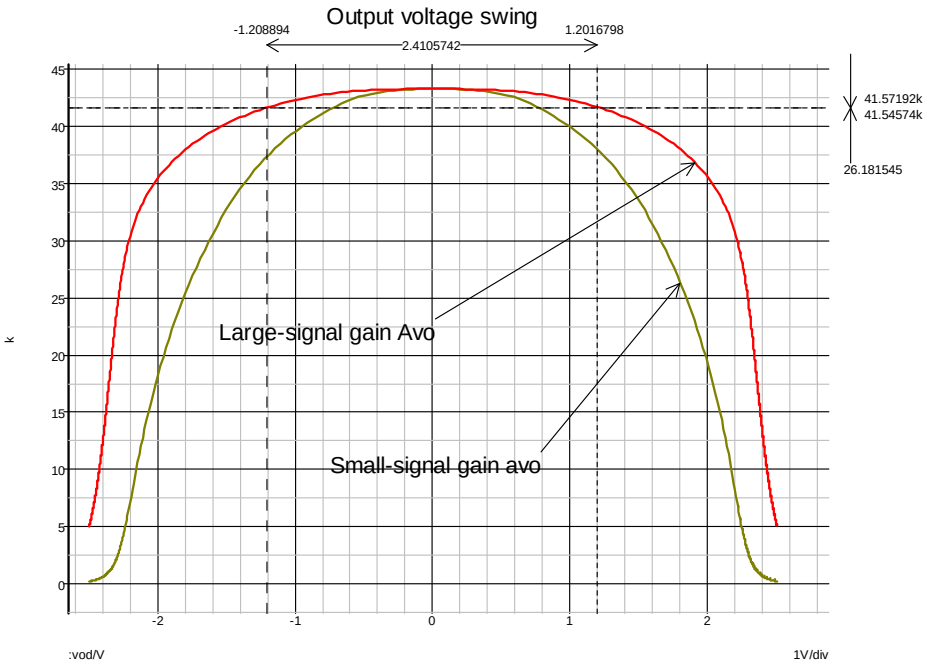
OTA design methodology

Final schematic for differential OTA



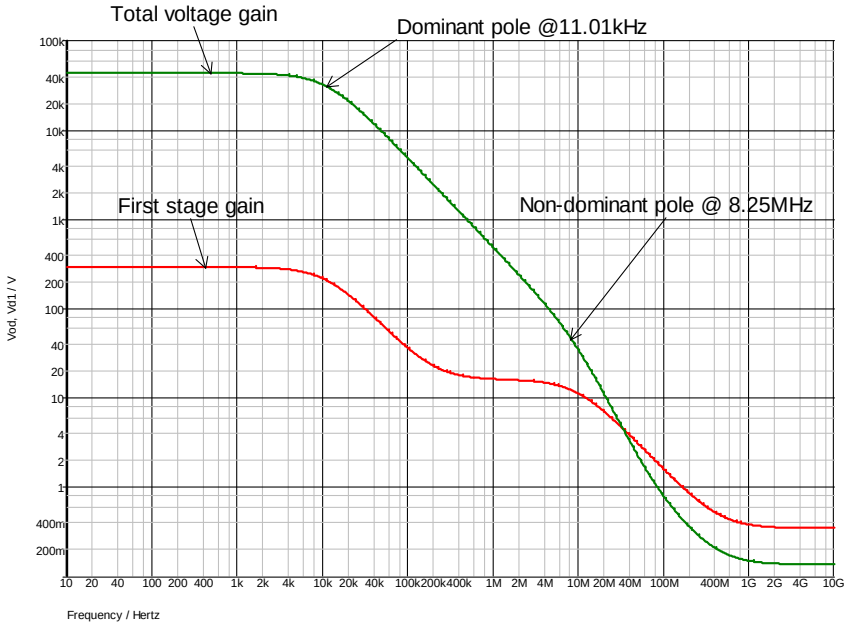
OTA Performance

Open-loop gain



Open-loop gain exceeds 40,000 for the operation range (2.4Vpk-pk)

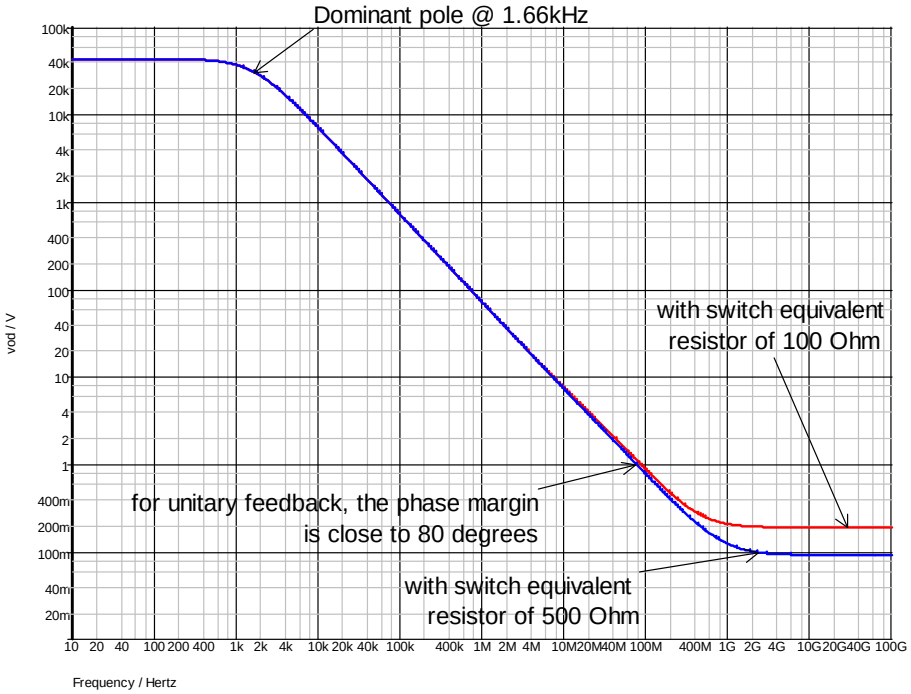
Frequency response



Dominant and non-dominant pole about three decade apart

OTA Performance

Frequency response with external compensation



Input differential capacitance

External compensation of 3pF yields phase margin of about 80 degrees

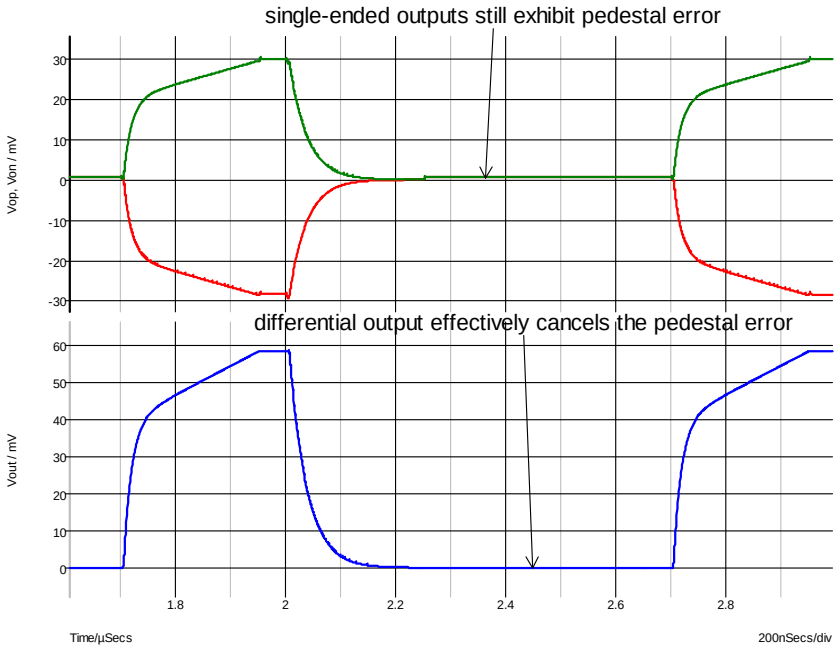
Compensation switch optimally sized for zero-nulling

Cin ~ 12pF at low frequencies

Decays for high frequencies because of absence of Miller effect

OTA Performance

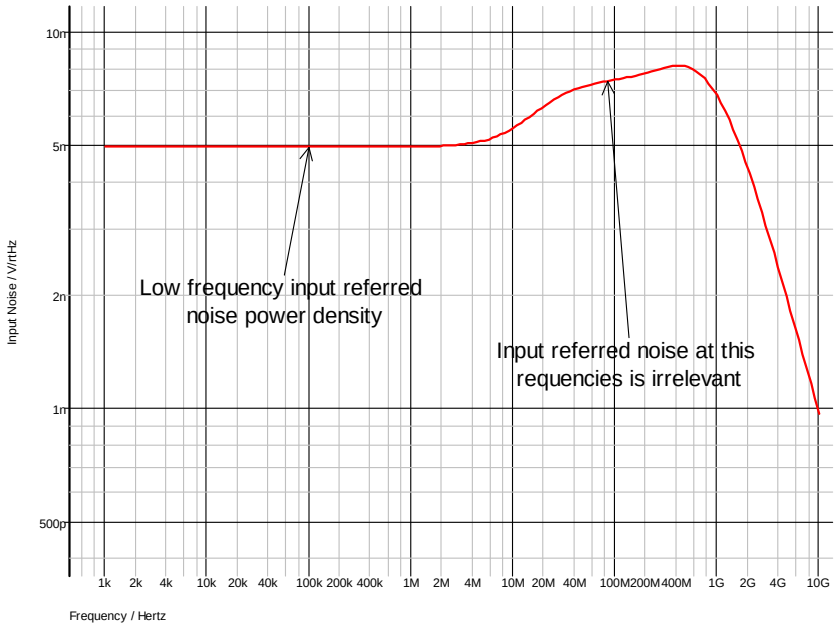
Transient response with external compensation



External compensation of 3pF effectively reduces differential transient ringing

CMFB amplifier is also compensated (1pF) to reduce common-mode voltage transient ringing

Input referred noise density

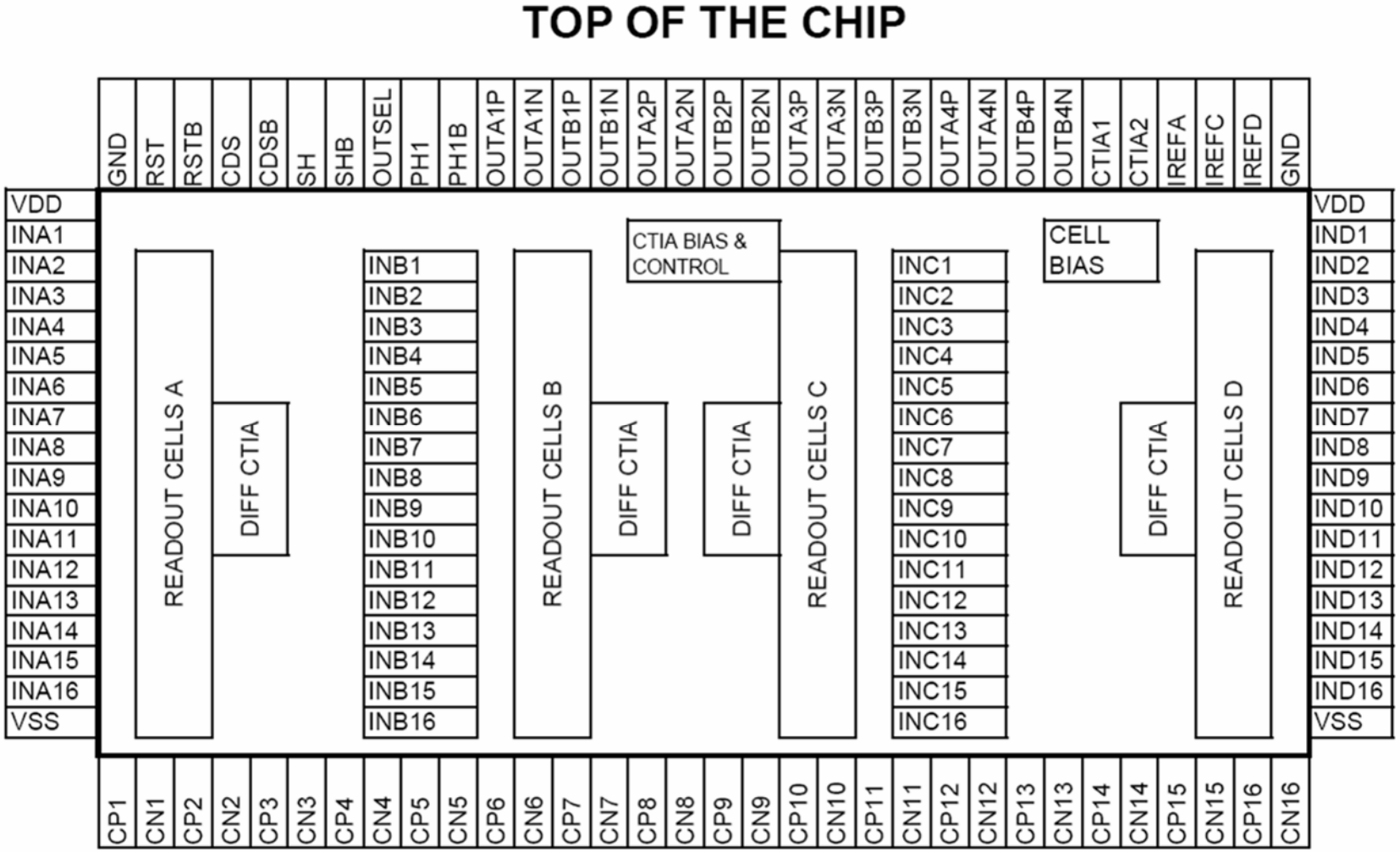


Low frequency input referred noise around 5nV/rtHz

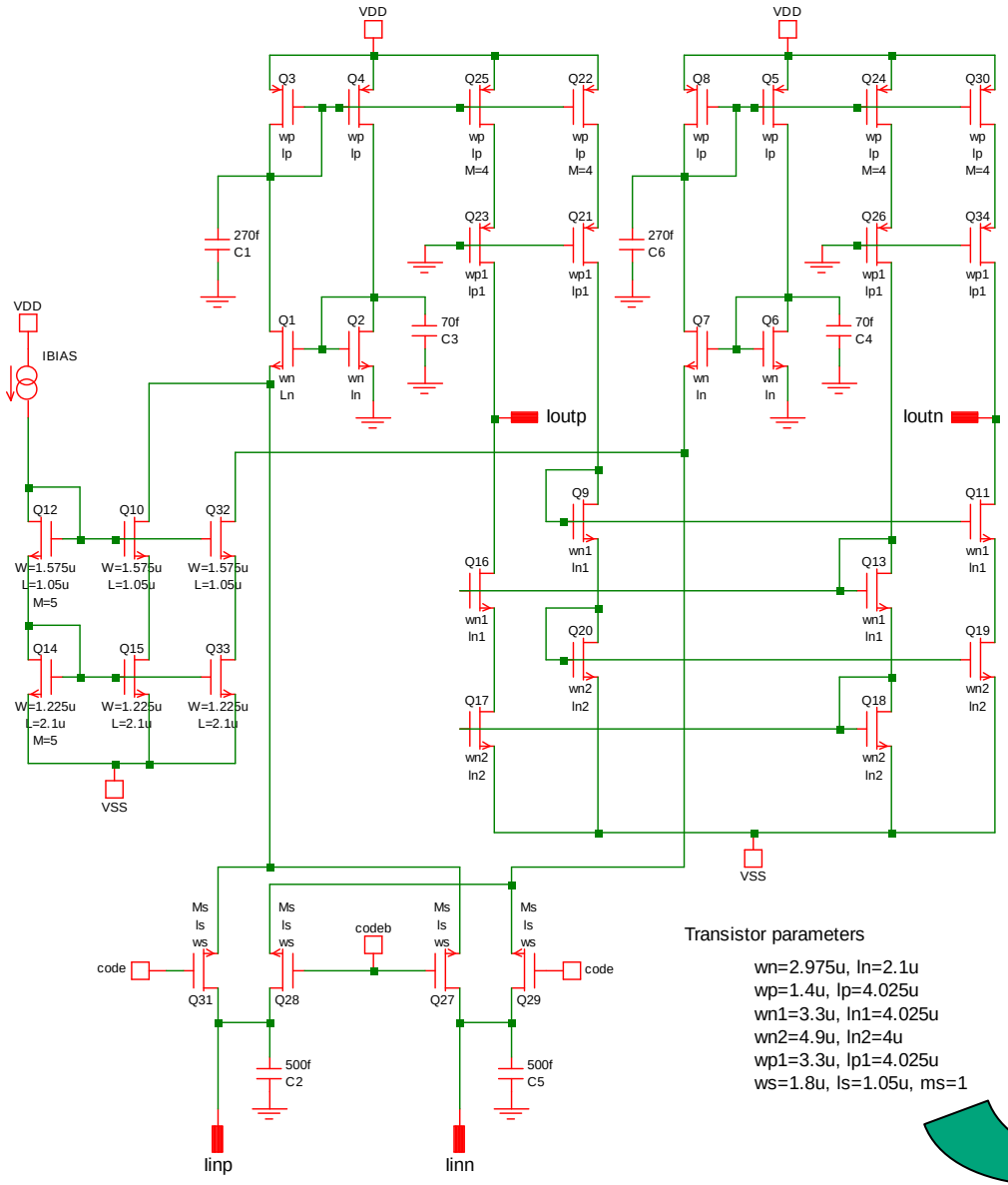
High frequency noise density is not relevant in this case

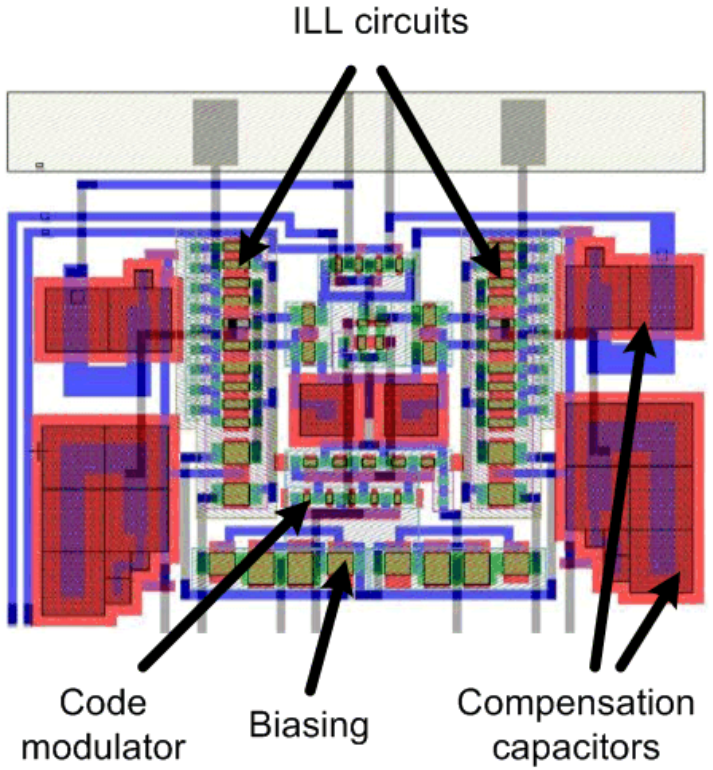
Second generation ROIC

Four 1x16 arrays + Fully differential CTIA



Readout cell physical design



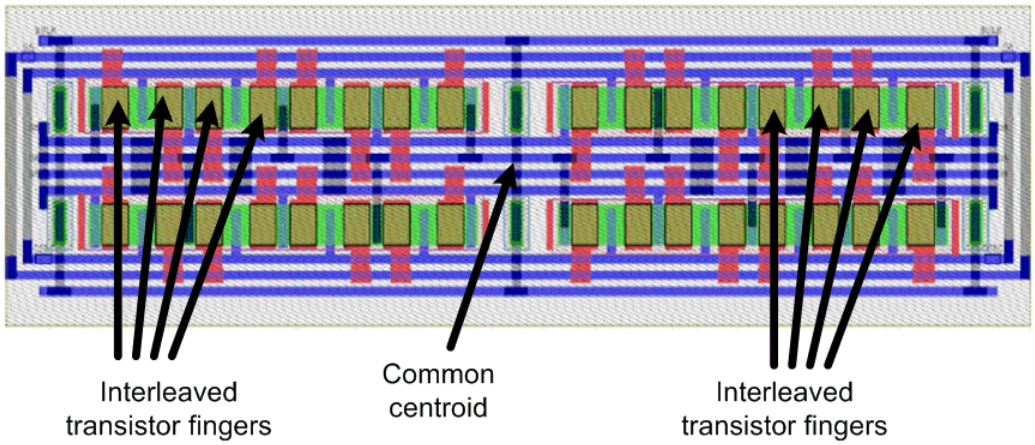


Transistor parameters

wn=2.975u, ln=2.1u
wp=1.4u, lp=4.025u
wn1=3.3u, ln1=4.025u
wn2=4.9u, ln2=4u
wp1=3.3u, lp1=4.025u
ws=1.8u, ls=1.05u, ms=1

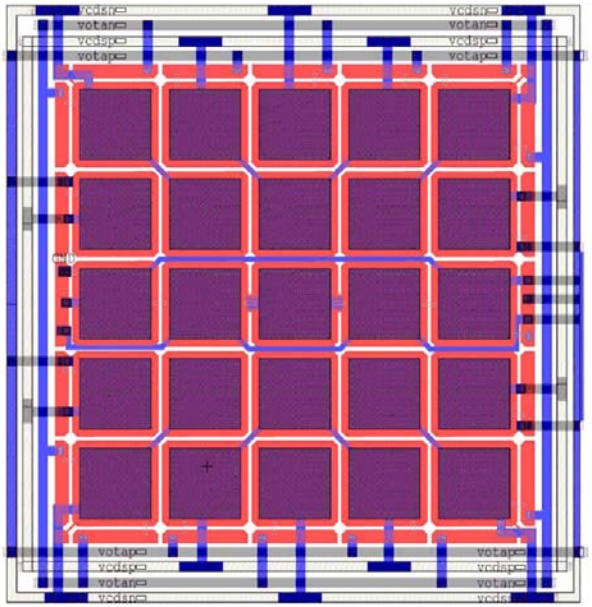
CTIA physical design

Matching transistors and capacitors



All differential pairs are designed with multi-finger, common-centroid structure

The differential OTA is divided into differential pair sections

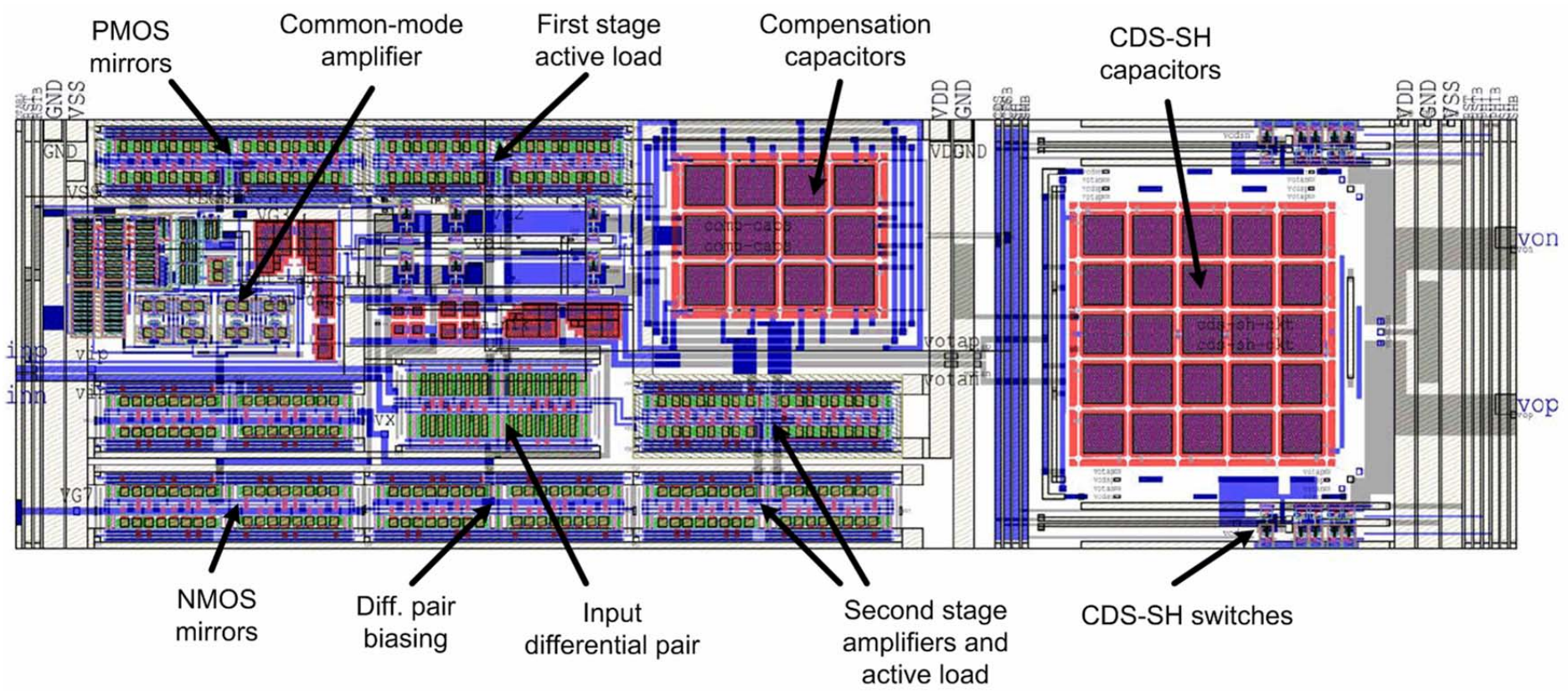


Four-capacitor layout using common-centroid techniques

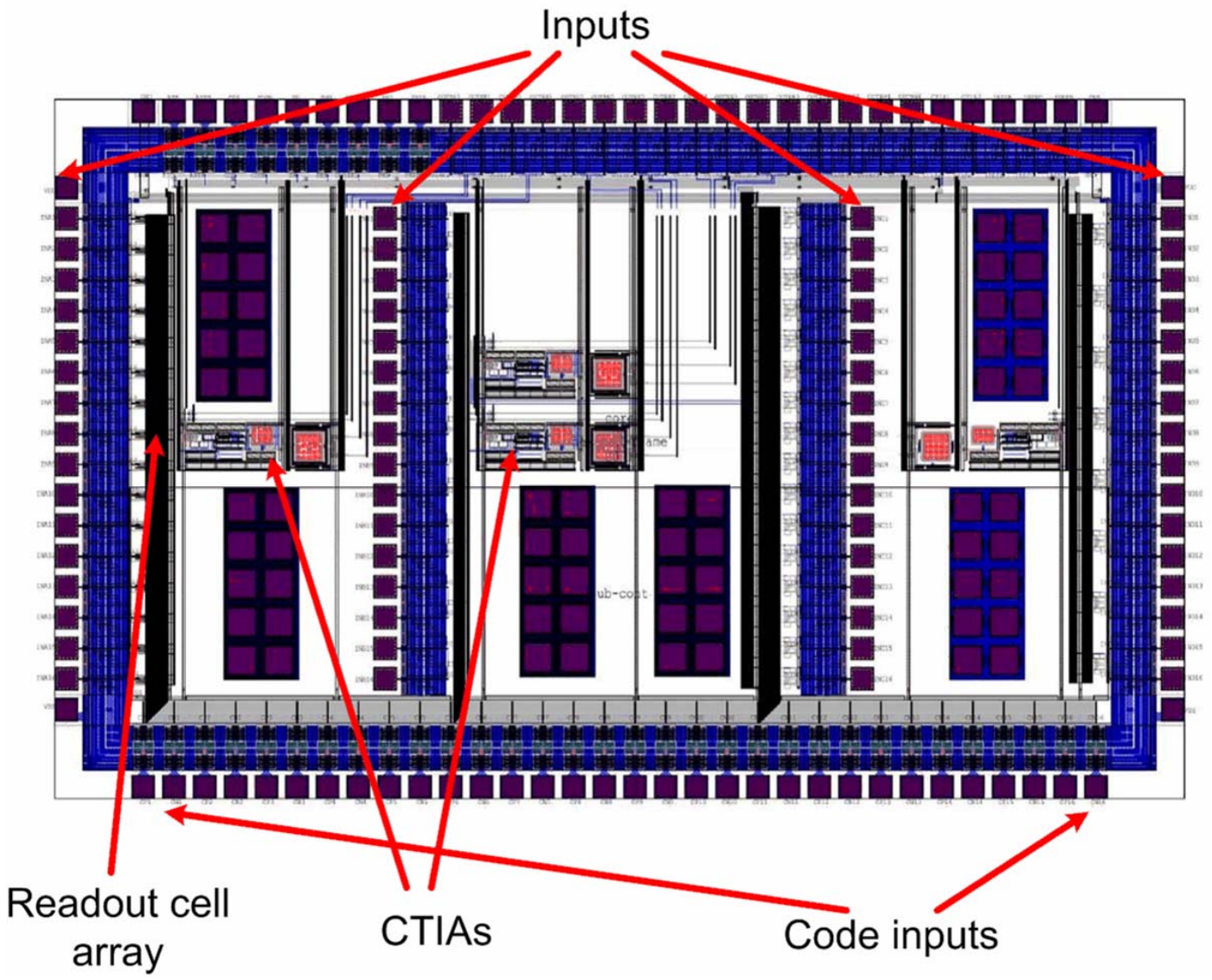
Dummy cap in the middle shorted to ground

ROIC physical design

Fully differential CTIA amplifier



ROIC physical design



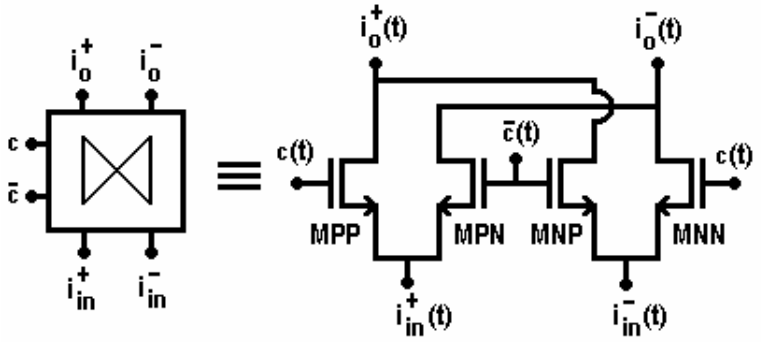
ORTHOGONALLY MODULATED CMOS READOUT INTEGRATED CIRCUIT FOR IMAGING APPLICATIONS

- Introduction and motivation
- Contribution Phase I: Proof of principle
  - Orthogonal encoding readout system description
  - Prototype system design and verification
  - Conclusions
- Contribution Phase II: Improving the system performance
  - Readout cell improvements
  - Transimpedance amplifier integration
- **Conclusion and brainstorm on further improvements**

Conclusion

Satisfactory results with the prototype experiment confirm validity of the orthogonal encoding scheme for readout circuits

Expect system performance improvement with the design optimization of the readout cell and the integration of the fully differential CTIA



$$i_o^+(t) = i_{in}^+(t)\cdot c(t) + n_c + i_{in}^-(t)\cdot \bar{c}(t) + n_{\bar{c}},$$

$$i_o^-(t) = i_{in}^+(t)\cdot \bar{c}(t) + n_{\bar{c}} + i_{in}^-(t)\cdot c(t) + n_c,$$

$$i_{od}(t) = i_o^+(t) - i_o^-(t) = [i_{in}^+(t) - i_{in}^-(t)]\cdot[c(t) - \bar{c}(t)],$$

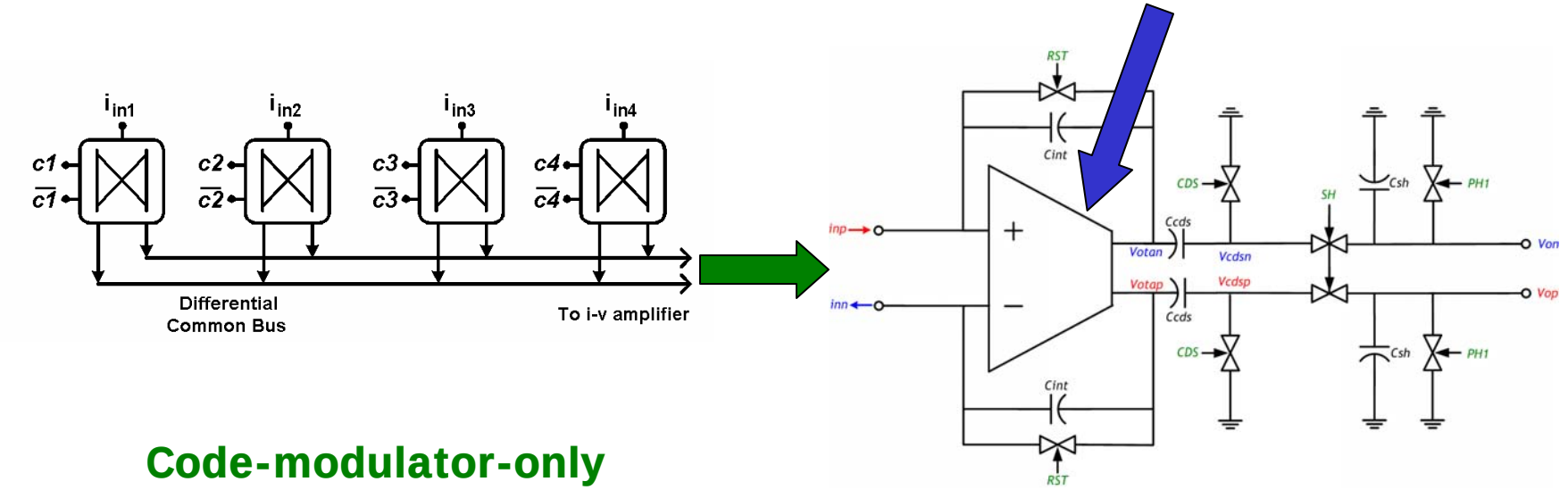
The readout cell with the code-modulator only is an outstanding candidate for highly-scalable imaging systems. Its characteristics: only four transistors, zero noise, no power consumption, no band width limitations.

Further improvement is accomplished if differential photodetector devices are used

Conclusion (cont'd)

Take advantage of switched nature of the system to cancel charge injection peaks from readout cells.

With code-modulator-only cells the system becomes highly-scalable but the noise performance of the OTA amplifier needs to be improved by one order of magnitude

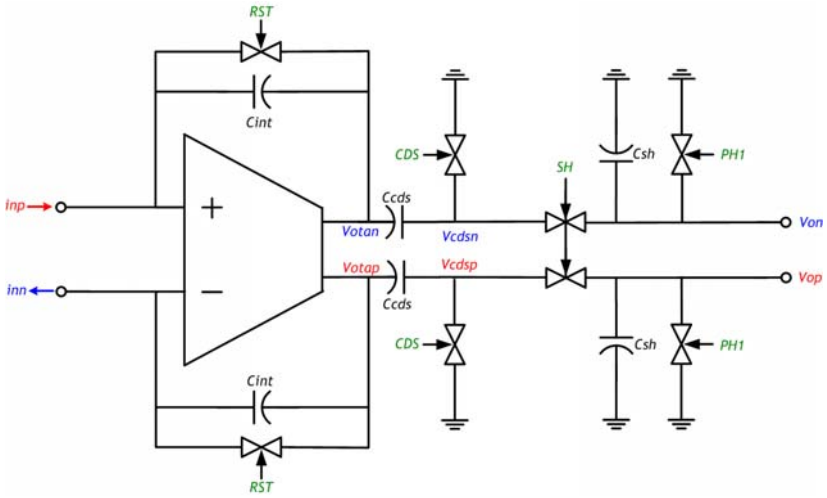


Code-modulator-only readout cell array

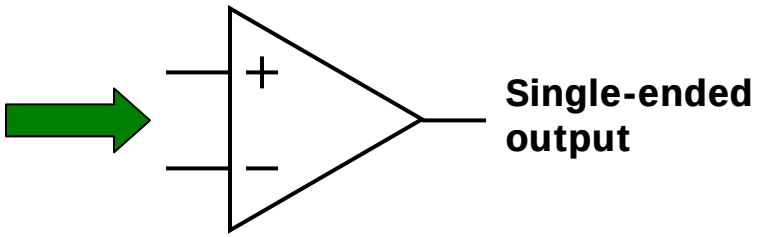
Capacitive Transimpedance amplifier per row

Conclusion (cont'd)

Integrating an amplifier to perform differential to single-ended conversion inside the chip would improve the system performance (pedestal voltages and vestigial voltage spikes would be cancelled inside the integrated circuit)



Capacitive Transimpedance amplifier per row



Differential amplifier per row

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